8장. 플립-플롭과 관련소자

- 래치 (1)
- 에지 트리거드 플립-플롭(2)
- 마스터-슬레이브 플립-플롭(3)
- 플립-플롭의 동작 특성(4)
- 플립-플롭의 응용(5)
- 원-샷(6)
- 555 타이머(7)

래치(Latches)

- 래치

  * 두 개의 안정된 상태를 갖는 임시 저장 장치

- S-R(Set-Reset) 래치

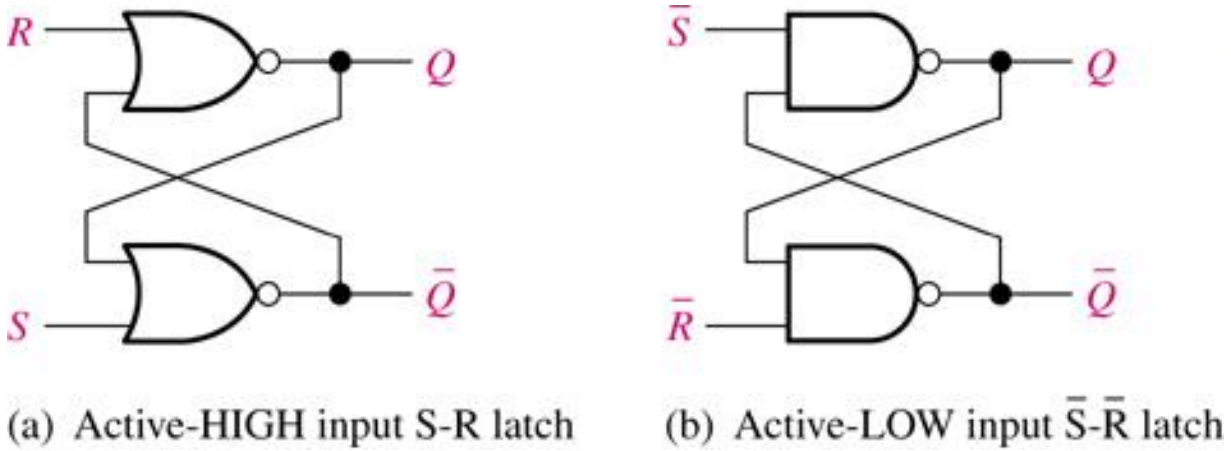
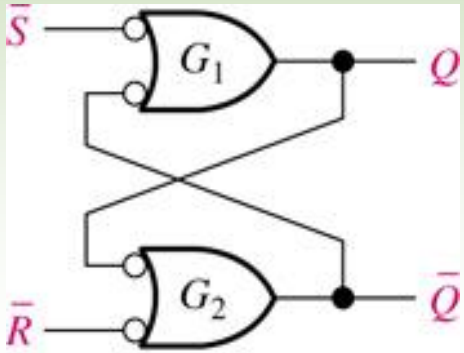


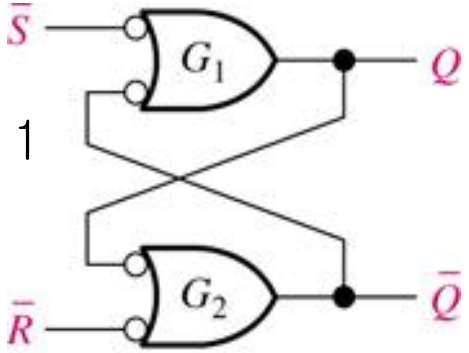
Figure 8-1 Two versions of SET-RESET (S-R) latches. Open file F08-01 and verify the operation of both latches.

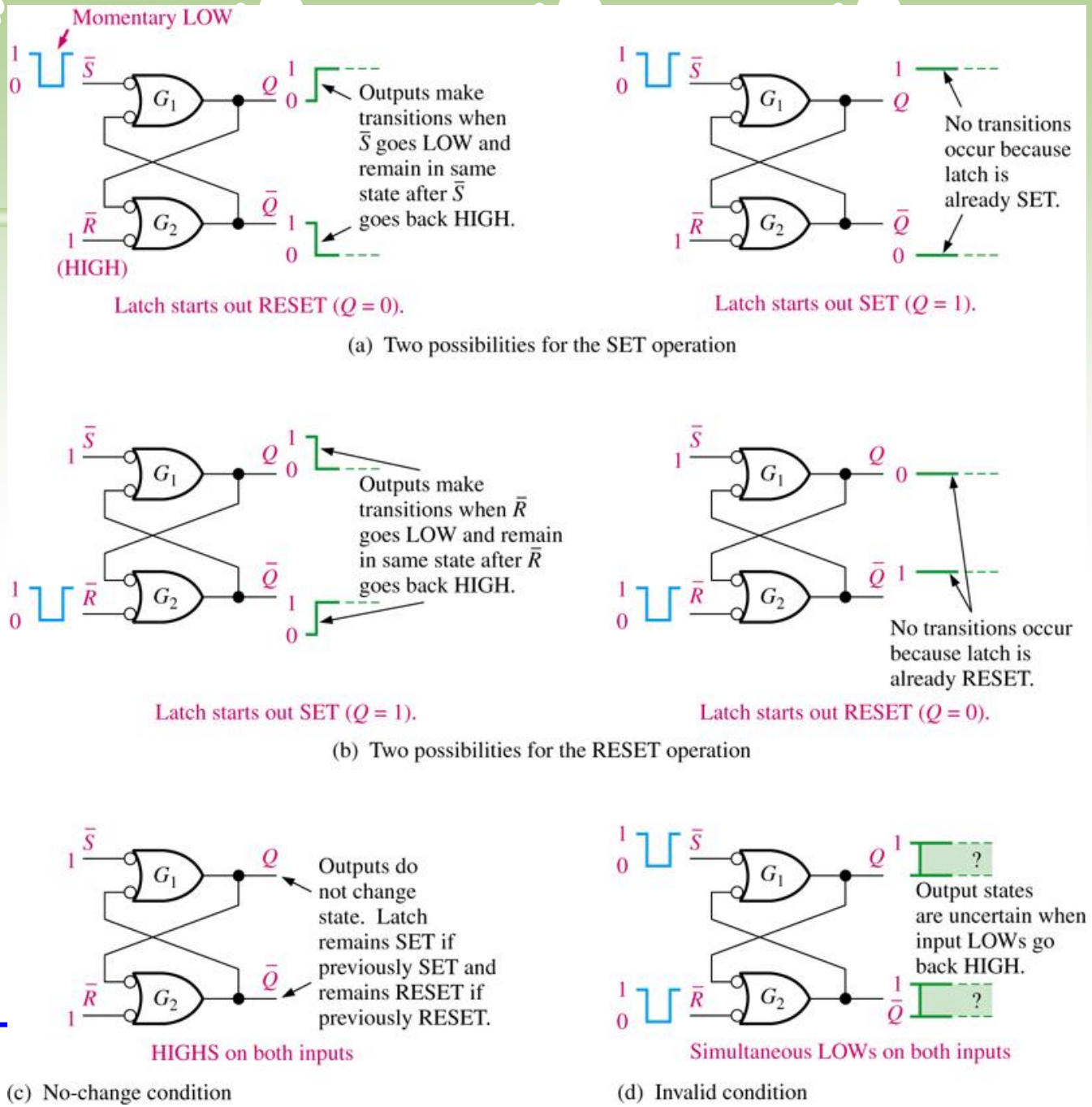
래치(Latches)

* 셋(Set) 상태 ;
  Q = 1



* 리셋(Reset) 상태 ;
  Q = 0




Momentary LOW
Outputs make transitions when $\overline{S}$ goes LOW and remain in same state after $\overline{S}$ goes back HIGH.
(HIGH)
Latch starts out RESET ($Q = 0$).
No transitions occur because latch is already SET.
Latch starts out SET ($Q = 1$).
(a) Two possibilities for the SET operation
Outputs make transitions when $\overline{R}$ goes LOW and remain in same state after $\overline{R}$ goes back HIGH.
Latch starts out SET ($Q = 1$).
No transitions occur because latch is already RESET.
Latch starts out RESET ($Q = 0$).
(b) Two possibilities for the RESET operation
Outputs do not change state. Latch remains SET if previously SET and remains RESET if previously RESET.
HIGHS on both inputs
(c) No-change condition
Output states are uncertain when input LOWs go back HIGH.
Simultaneous LOWs on both inputs
(d) Invalid condition

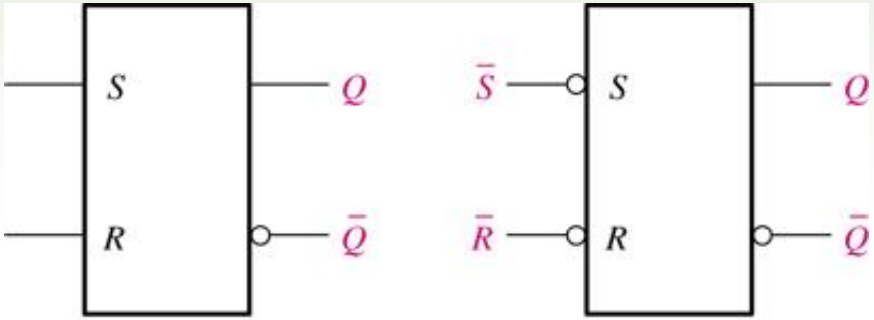
래치 (1)

래치(Latches)

* Active Low 입력 S′–R′ 래치의 진리표

Inputs S′	R′	Output Q	Q′	Comments
1	1	NC	NC	
0	1	1	0	
1	0	0	1	
0	0	1	1	

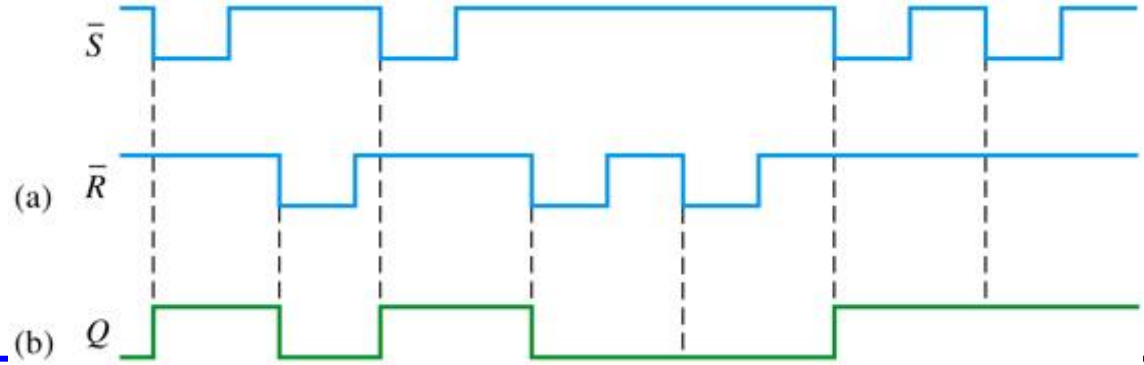
* 논리 기호



(a) Active-HIGH input S-R latch

(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

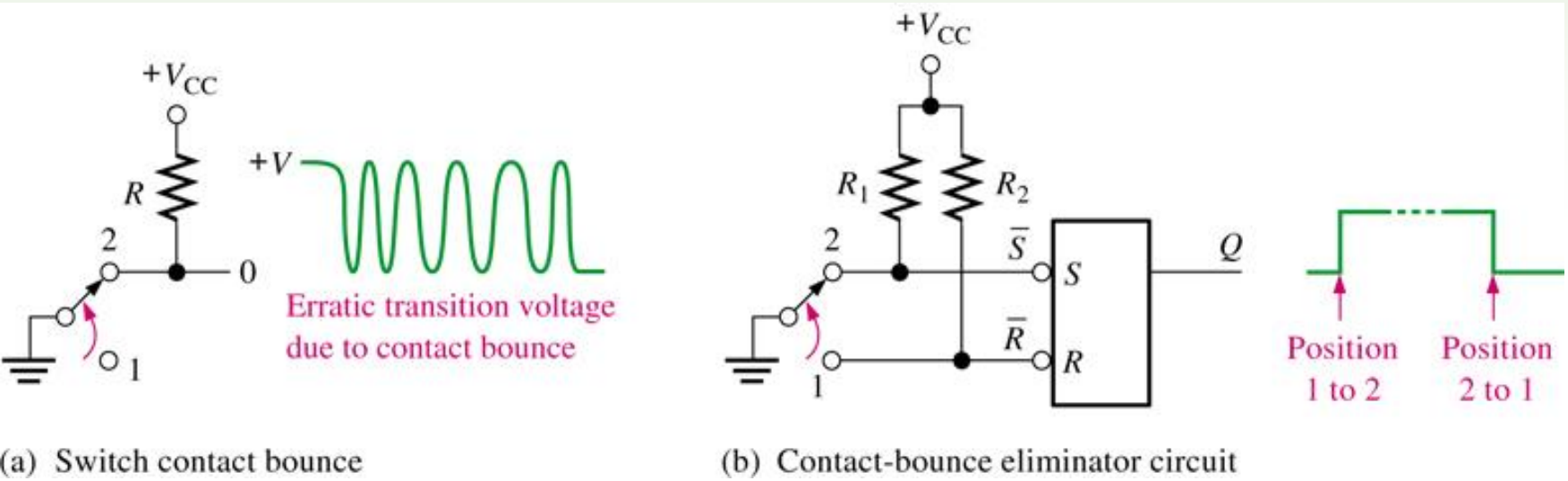
* 예제 8-1)
Active Low 입력 S′–R′ 래치



래치(Latches)

- 응용 문제

* 접촉 바운스 제거용으로 사용된 래치

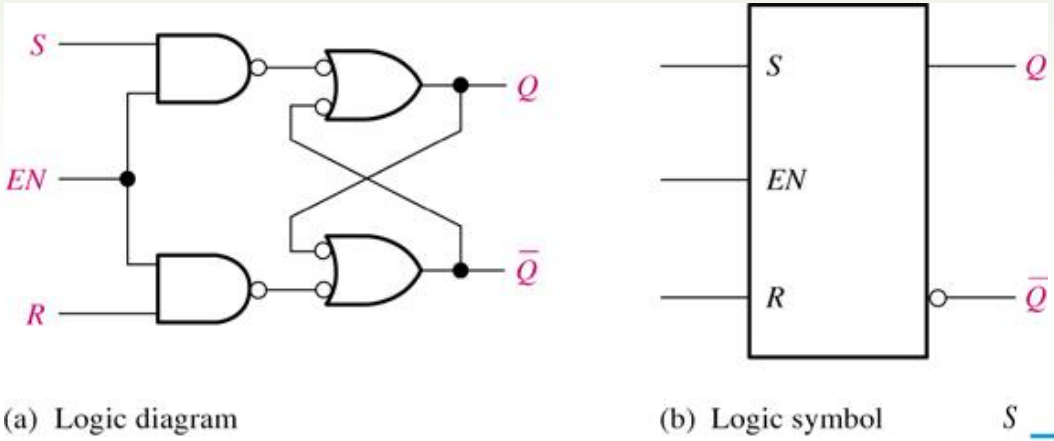


(a) Switch contact bounce

(b) Contact-bounce eliminator circuit

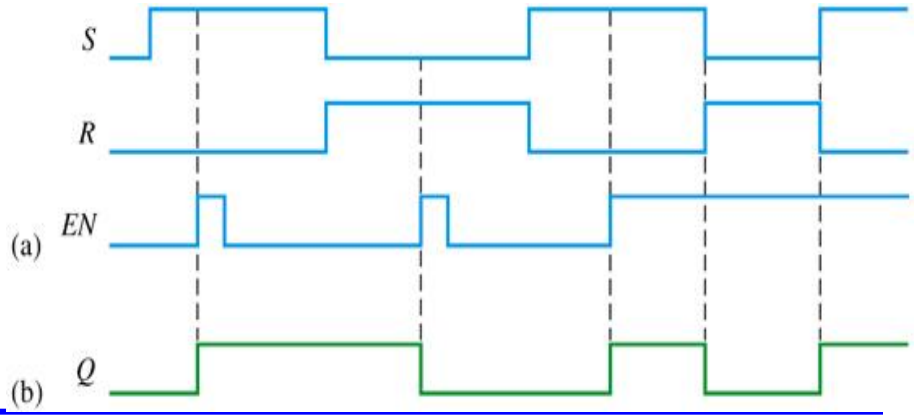
래치(Latches)

- 게이티드 S-R 래치



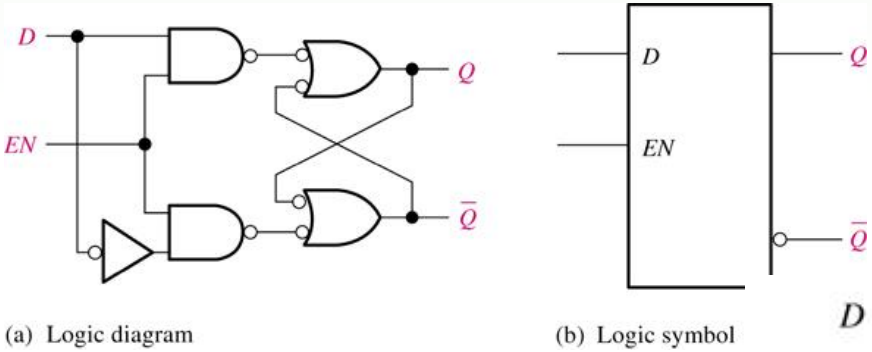
(a) Logic diagram (b) Logic symbol

* 예제 8-2) 초기에 리셋상태



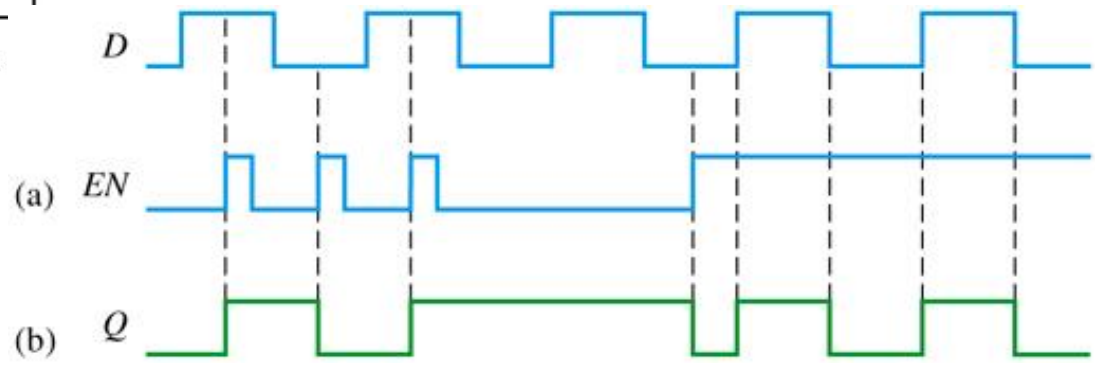
래치(Latches)

- 게이티드 D 래치
  - 입력 D가 HIGH, EN이 HIHG 일 때, 래치는 셋
  - 입력 D가 LOW, EN이 HIHG 일 때, 래치는 리셋



(a) Logic diagram (b) Logic symbol

* 예제 8-3) 초기에 리셋상태



에지 트리거드 플립-플롭

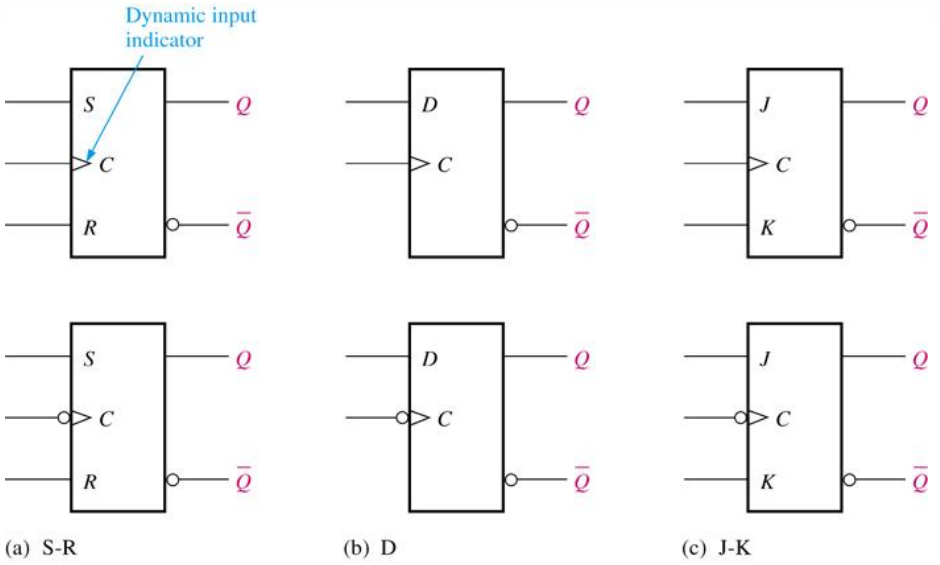
- 플립-플롭

* 동기식의 쌍안정 소자 ;

=>

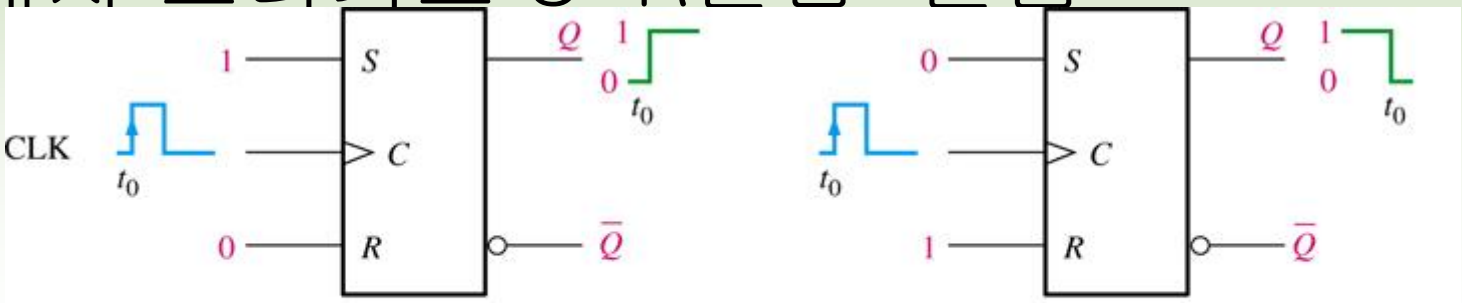
=> 2개의 안정된 상태를 가지기 때문에 기억소자로 사용 가능

* 에지 트리거드 플립-플롭 :



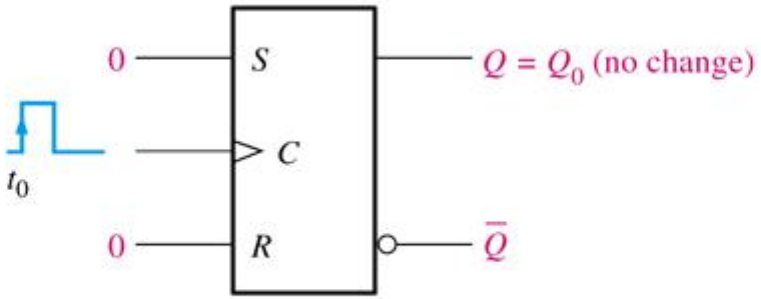
에지 트리거드 플립-플롭

- 에지 트리거드 S-R플립-플롭



(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $S = 0, R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0, R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

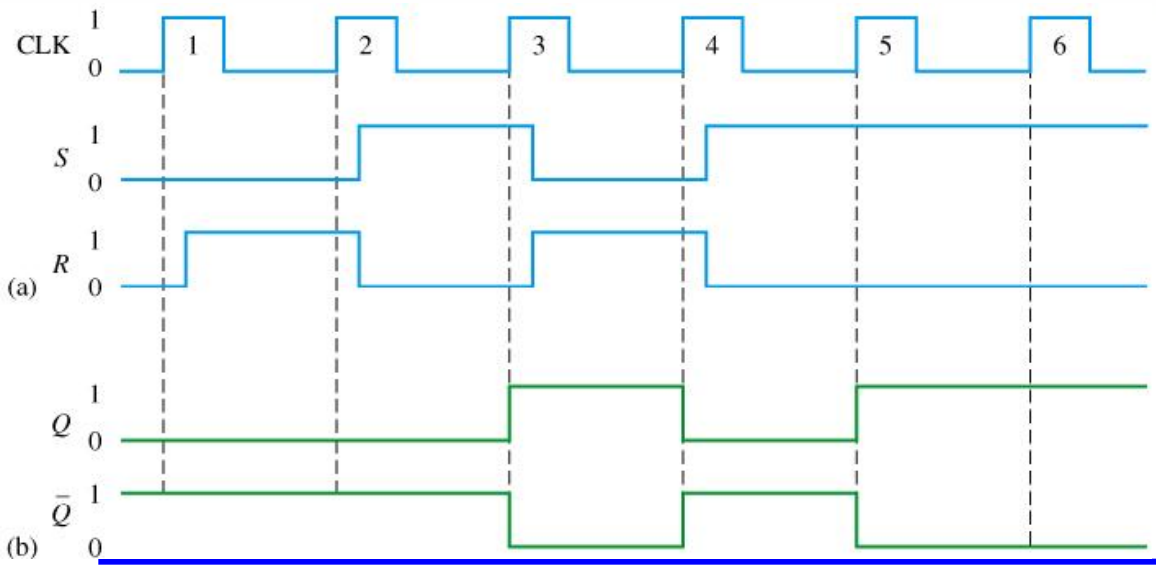
에지 트리거드 플립-플롭

에지 트리거드 S-R플립-플롭

진리표

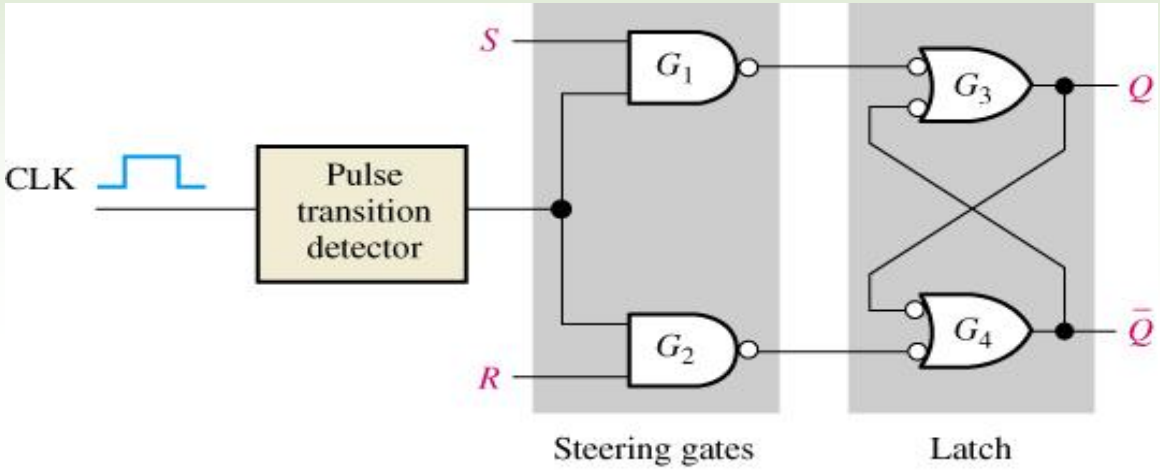
Input S	Input R	Output Q	Output Q′	Comments
0	0	Q	Q′	No change
0	1	0	1	Reset
1	0	1	0	Set
1	1	?	?	Invalid

* 예제 8-4) 상승 에지 트리거, 초기에 리셋상태

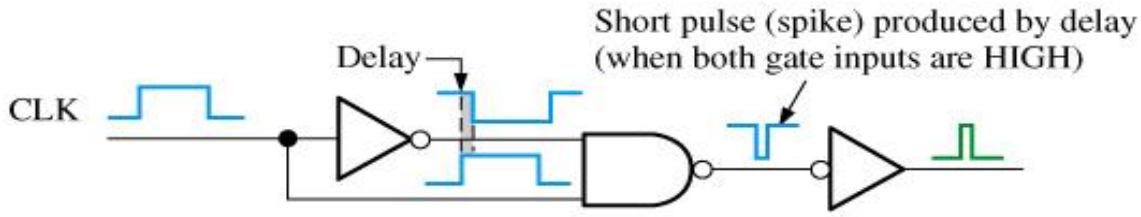


에지 트리거드 플립-플롭

- 에지 트리거링 방법



(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop



(b) A type of pulse transition detector

에지 트리거드 플립-플롭

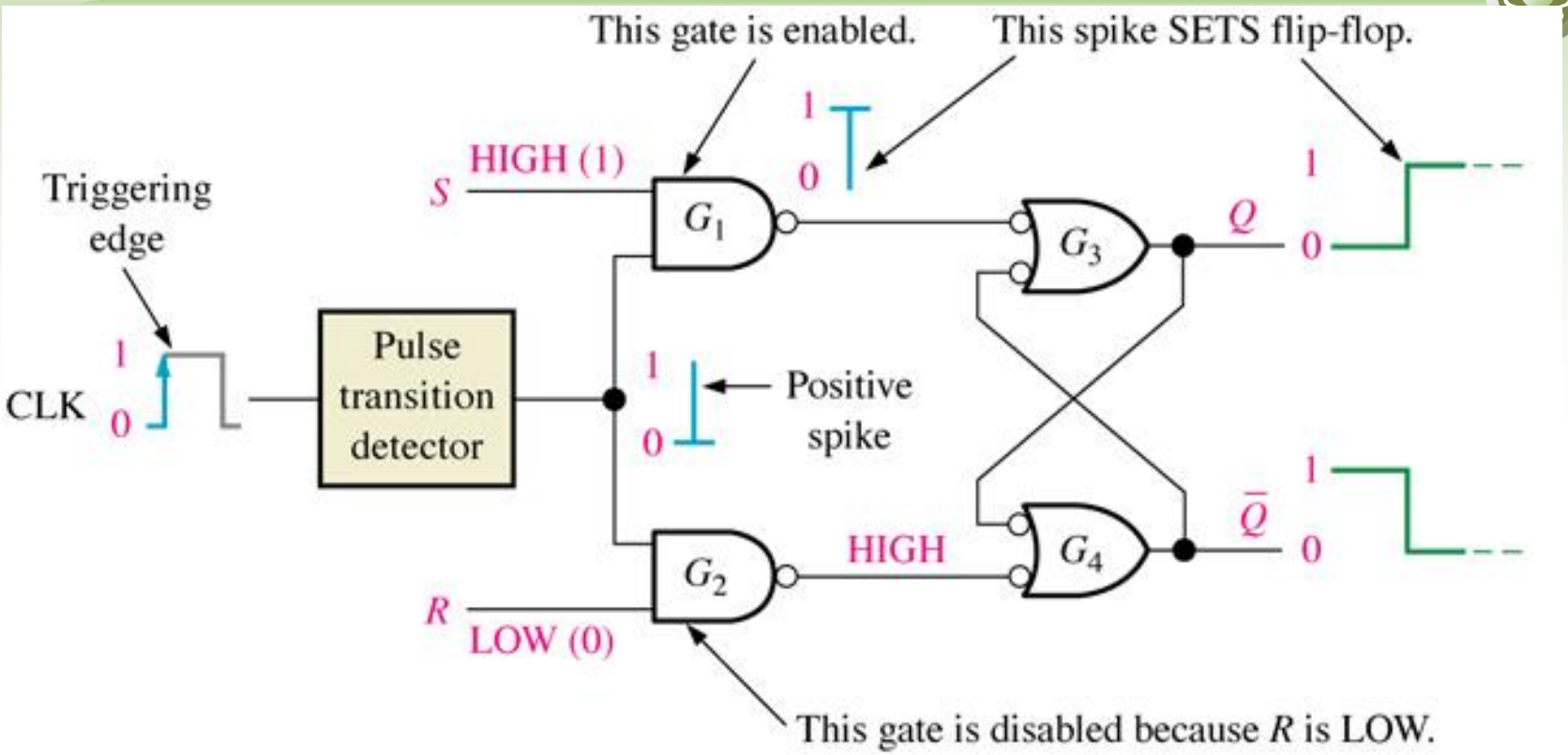


Figure 8-16 Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

에지 트리거드 플립-플롭

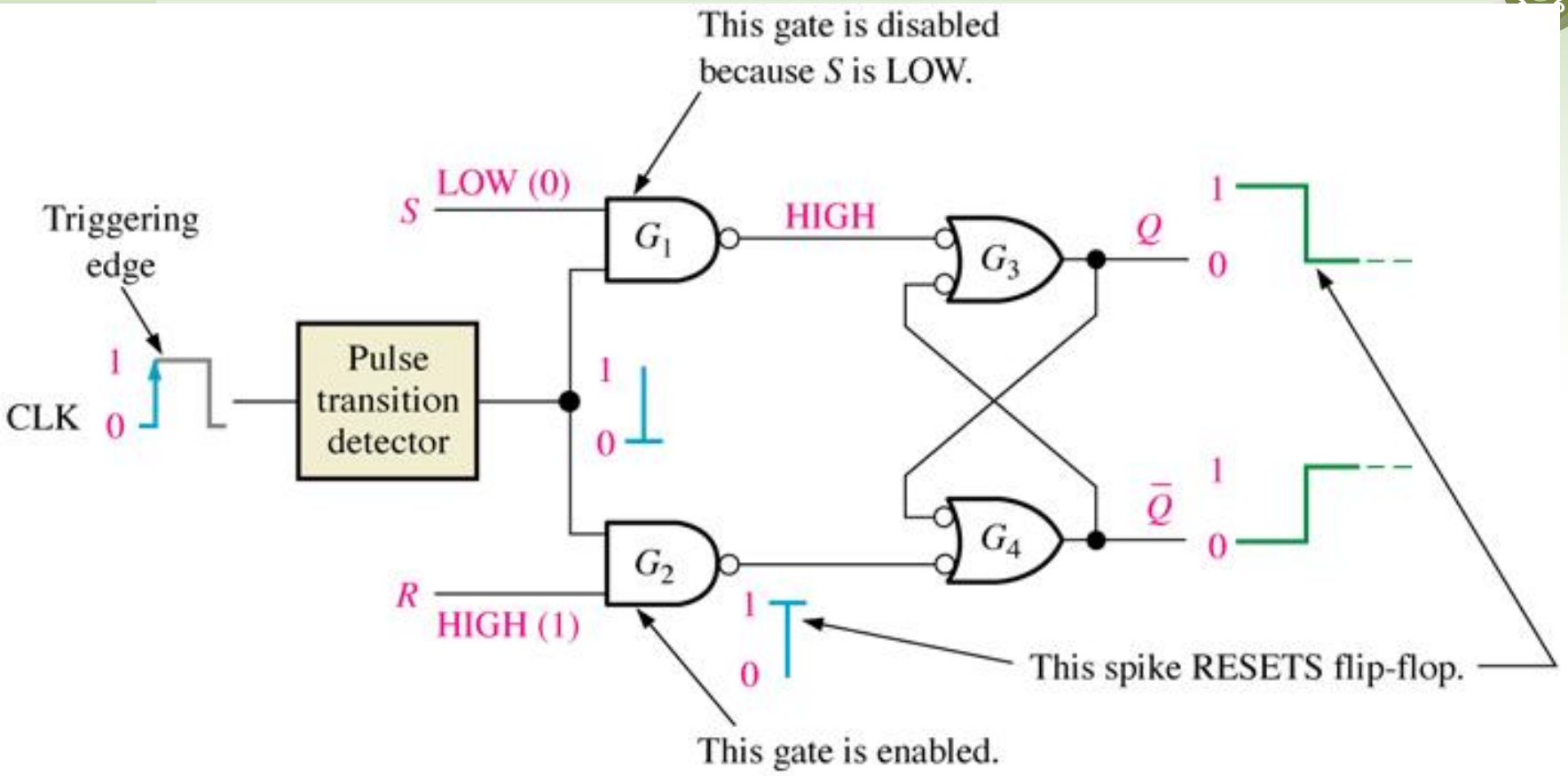
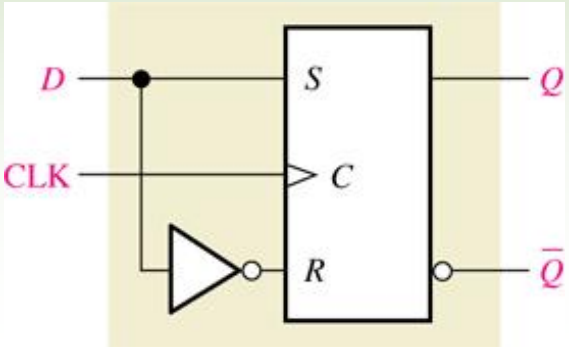


Figure 8-17 Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.

에지 트리거드 플립-플롭

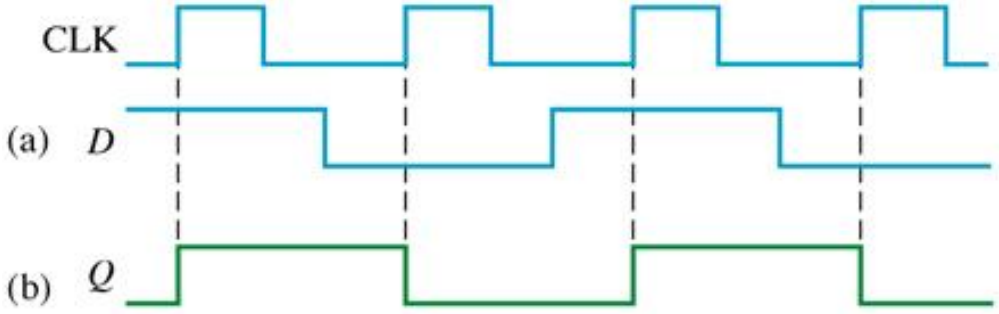
- 에지 트리거드 D 플립-플롭

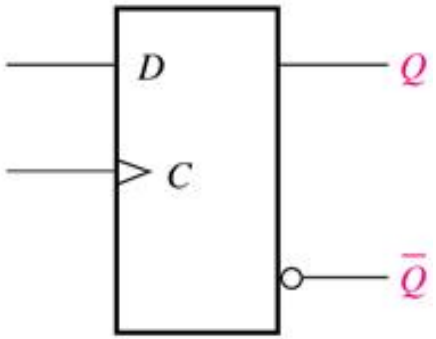


진리표

Inputs D	Inputs Clk	Outputs Q	Outputs Q′	Comments
0	↑	0	1	Reset
1	↑	1	0	Set

* 예제 8-5) 초기에 리셋상태





에지 트리거드 플립-플롭

- 에지 트리거드 J-K 플립-플롭

  * Set, Reset, No change 모드에서는 S-R 플립-플롭과 동작이 같다.

  * Invalid 대신 Toggle 모드가 있다.

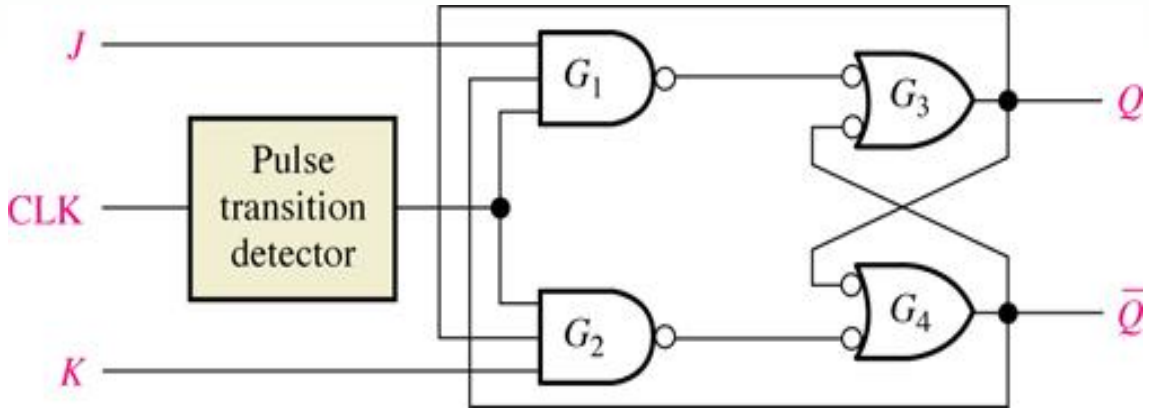


Figure 8-20 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

에지 트리거드 플립-플롭

* 초기에 플립-플롭은 리셋 상태(Q = 0)이고, J=1, K=0.
  => 클럭 펄스 ①이 가해지면,

* 리셋 상태에서 J=0, K=0로 하면,
* 리셋 상태에서 J=1, K=1로 하면,
* 셋 상태에서 J=1, K=1로 하면,
* J=1, K=1 =>

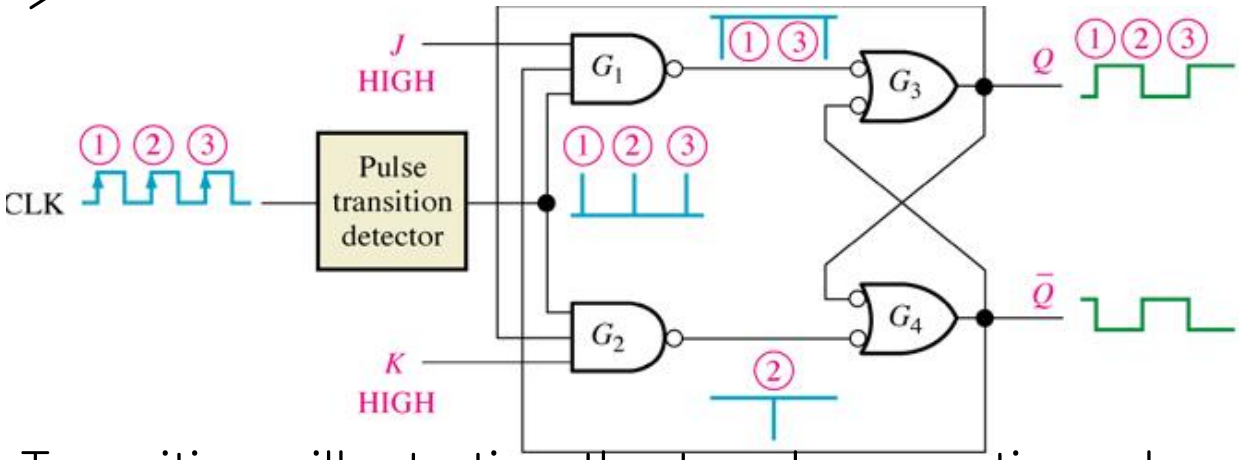


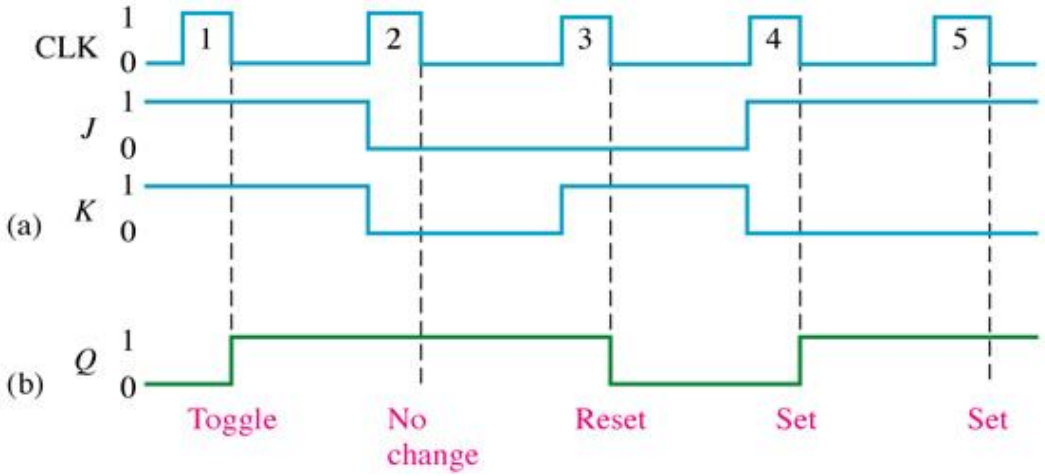
Figure 8-21 Transitions illustrating the toggle operation when J=1 and K=1.

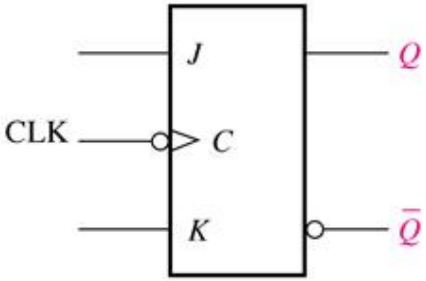
에지 트리거드 플립-플롭

* 상승 에지 트리거드
  J-K 플립-플롭의 진리표

Inputs J	K	Clk	Outputs Q	Q′	Comments
0	0	↑	Q	Q′	
0	1	↑	0	1	
1	0	↑	1	0	
1	1	↑	Q′	Q	

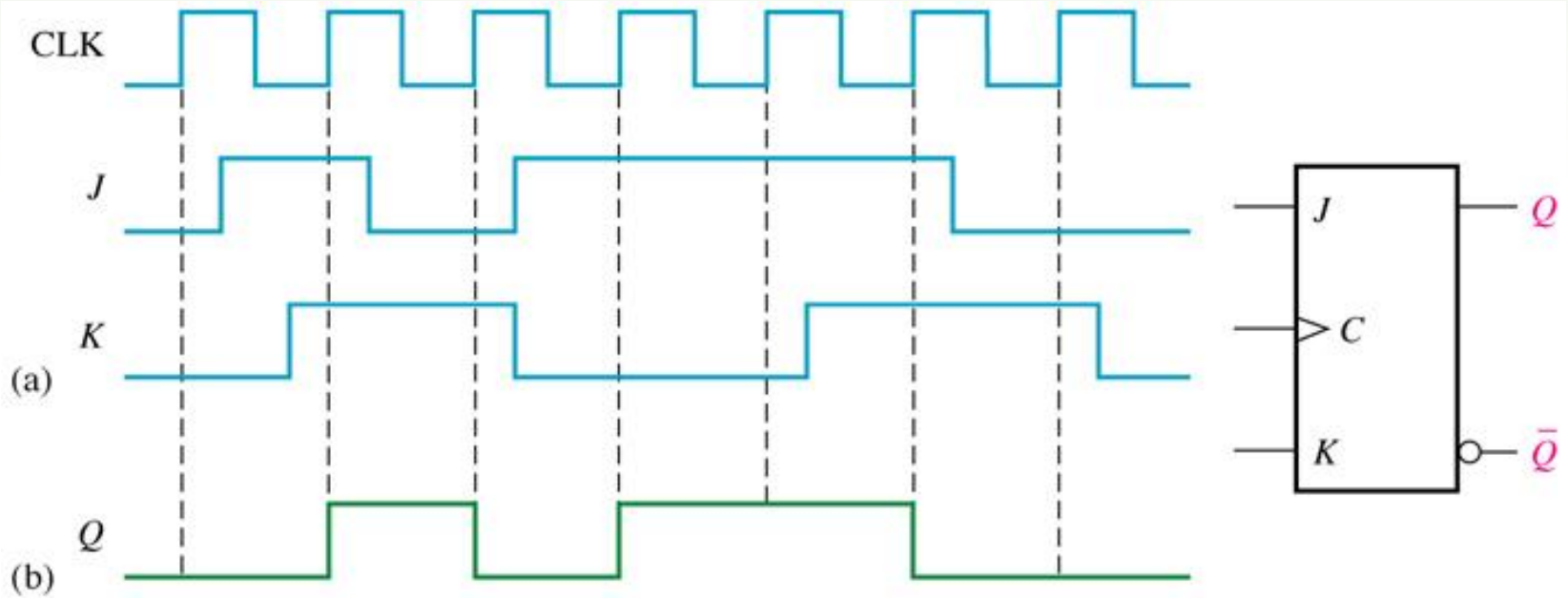
* 예제 8-6) 초기 리셋 상태





에지 트리거드 플립-플롭

* 예제 8-7) 초기 리셋 상태



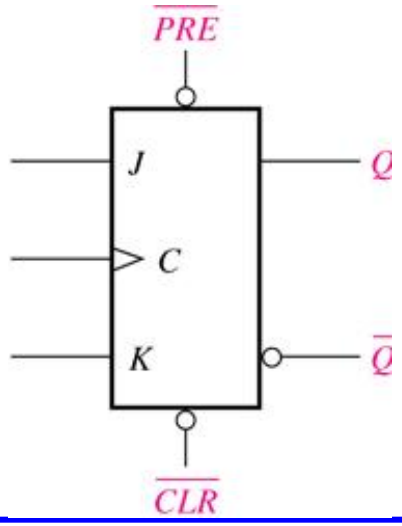
에지 트리거드 플립-플롭

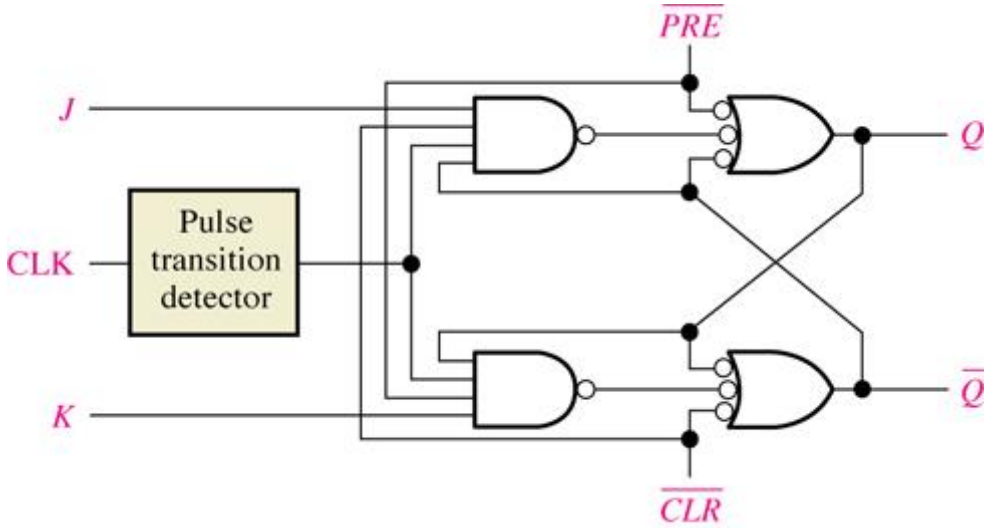
비동기식 프리셋 및 클리어 입력

* 비동기식 입력 : 클럭과 무관하게(Asynchronous) 플립-플롭의 상태에 영향을 준다.

* 프리셋(Preset), 직접 셋(direct set) : 플립-플롭을 셋 시키는 입력

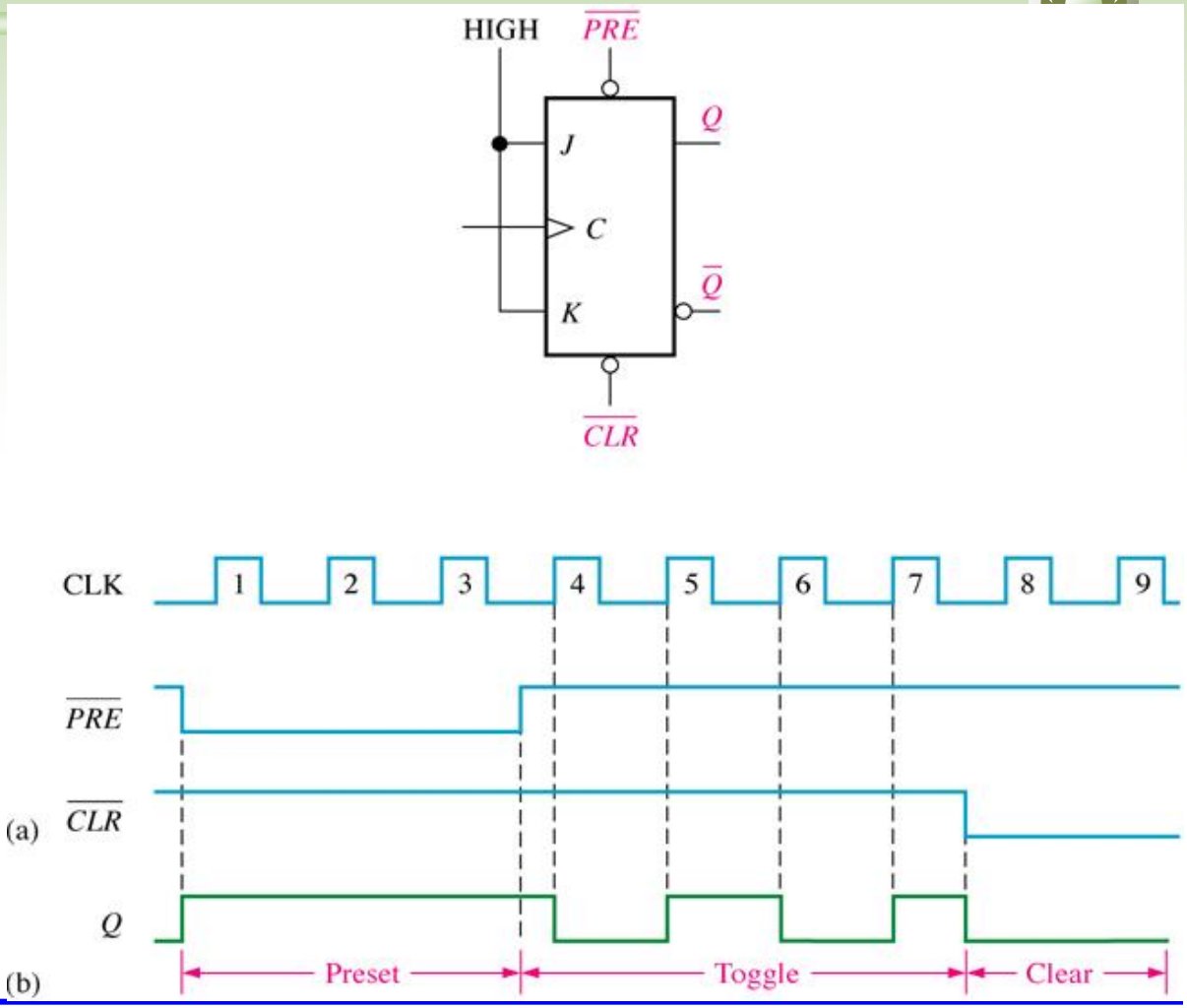
* 클리어(clear), 직접 리셋(direct reset) : 플립-플롭을 리셋 시키는 입력





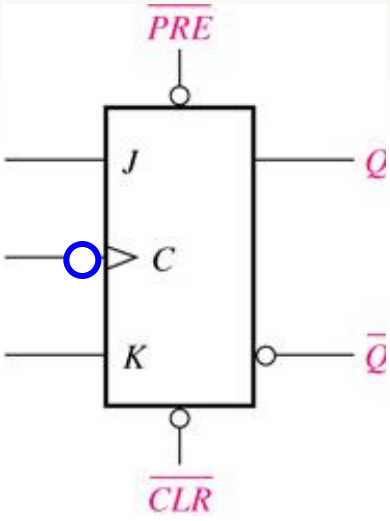
에지 트리거드 플립-플롭

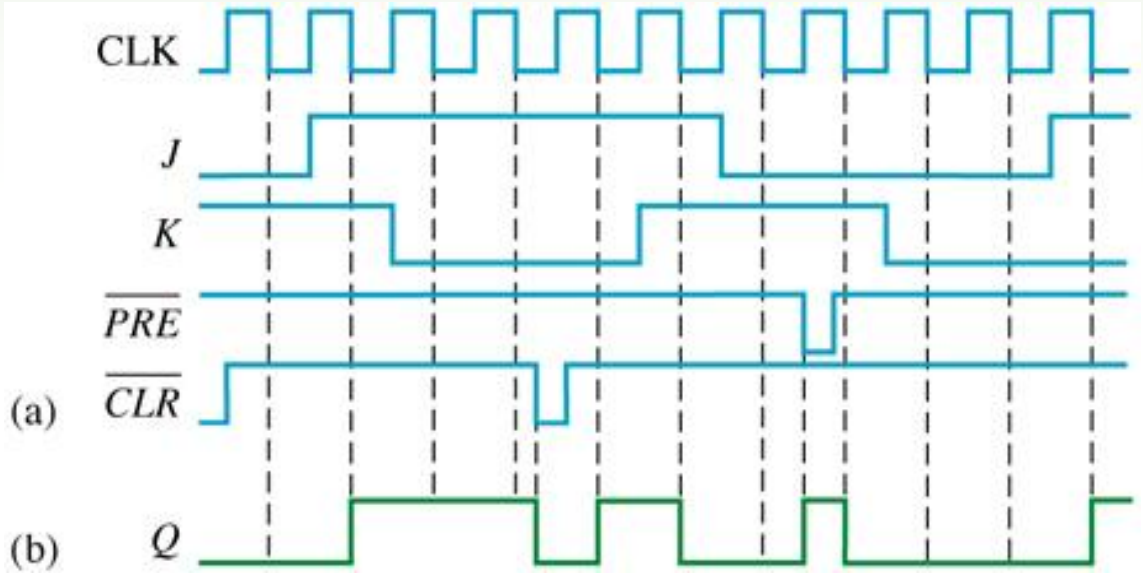
* 예제 8-8)
  프리셋 및 클리어



에지 트리거드 플립-플롭

* 예제 8-8) 하강 에지 트리거드 J-K 플립-플롭, 프리셋 및 클리어





마스터-슬레이브 플립-플롭

◉ 펄스-트리거드 마스터-슬레이브 플립-플롭

* 마스터 섹션의 상태 값은 클럭 펄스의
  상승 에지에서 J, K 값에 따라 결정 됨.

* 슬레이브 섹션의 상태 값은 클럭 펄스의
  하강 에지에서 마스터 섹션의 상태 값에 따라 결정 됨

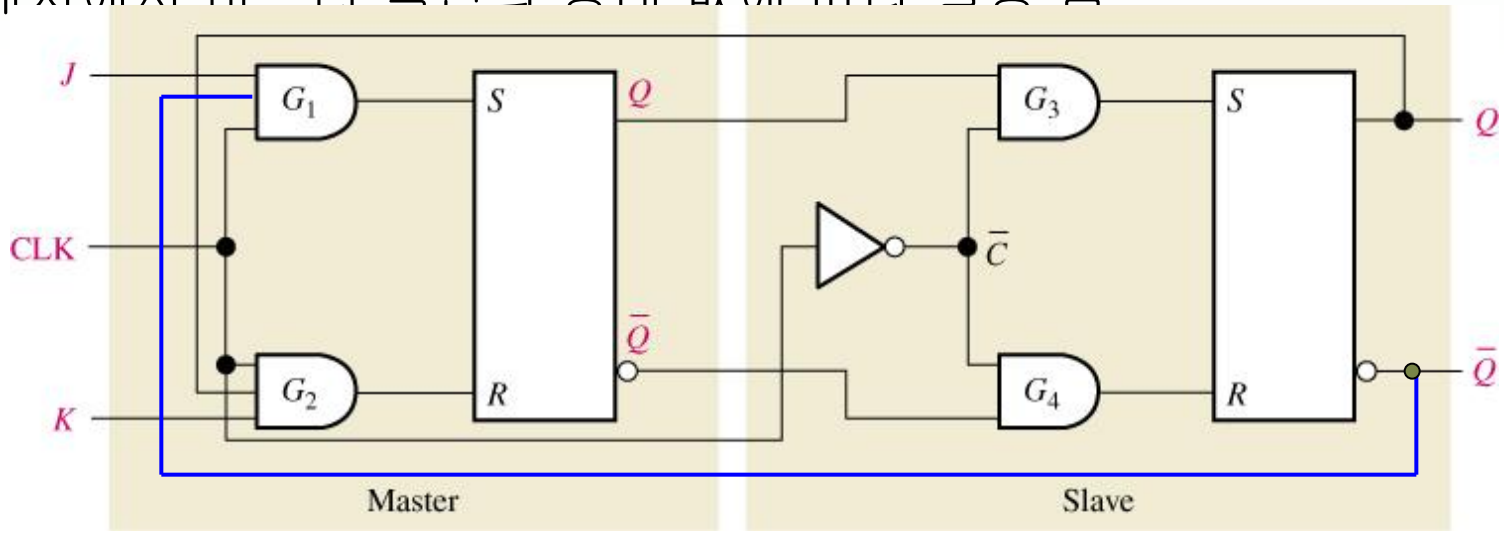


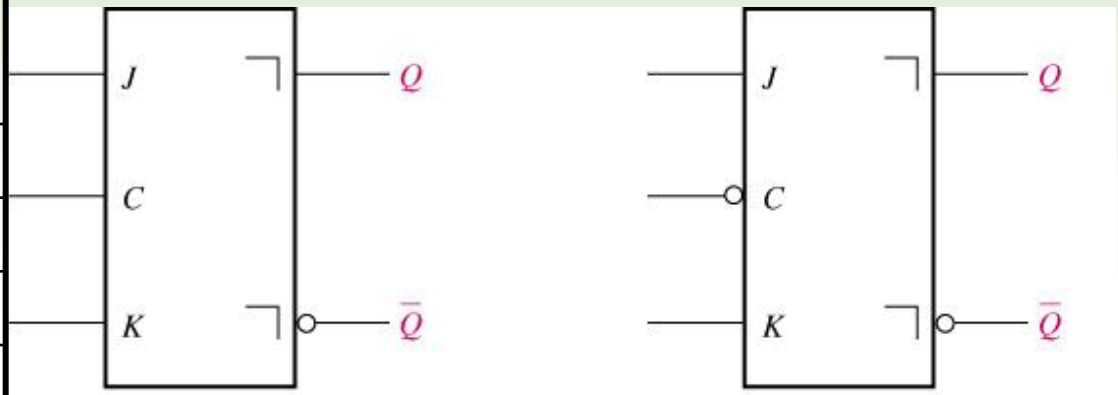
Figure 8-28 Basic logic diagram for a master-slave J-K flip-flop.

마스터-슬레이브 플립-플롭

* 진리표

Input J	K	Clk	Output Q	Q′	Comments
0	0	⎍	Q	Q′	
0	1	⎍	0	1	
1	0	⎍	1	0	
1	1	⎍	Q′	Q	

* 논리 기호

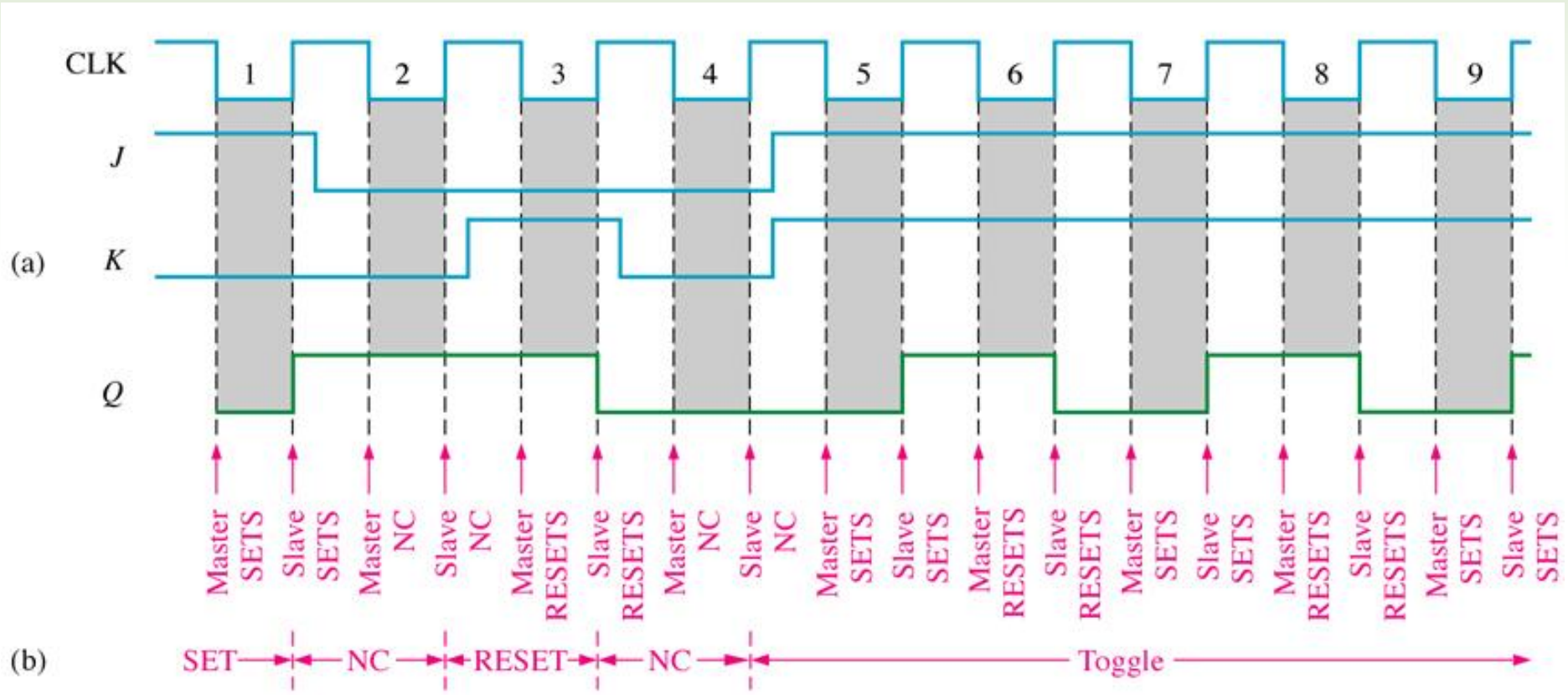


(a) Active-HIGH clock: Data are clocked in on positive-going edge of clock pulse and transferred to output on the following negative-going edge.

(b) Active-LOW clock: Data are clocked in on negative-going edge of clock pulse and transferred to output on the following positive-going edge.

마스터-슬레이브 플립-플롭

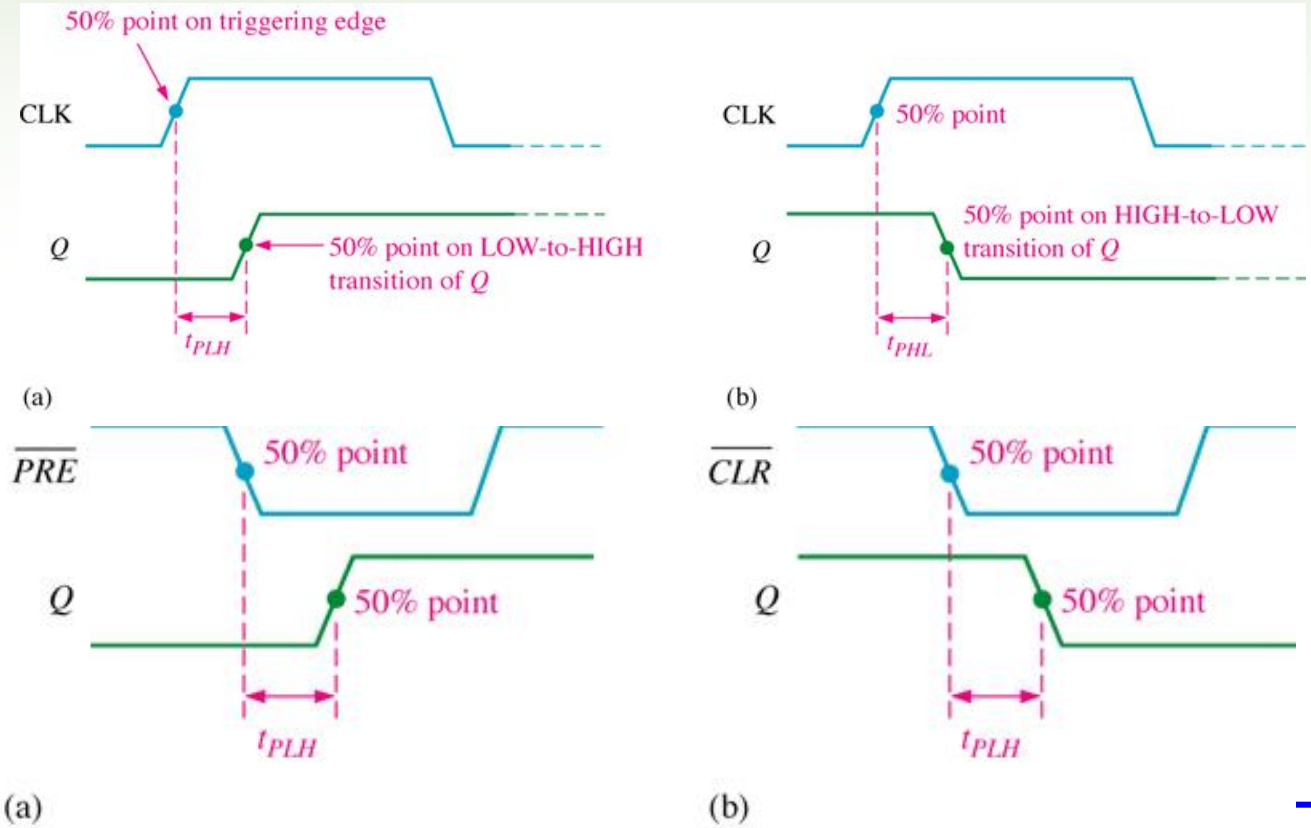
* 예제 8-10) 초기 리셋 상태, 클럭은 Active Low



플립-플롭의 동작 특성

- 전파 지연 시간(Propagation Delay Times)

* 입력신호가 가해진 후 출력의 변화가 발생할 때 까지의 지연 시간



플립-플롭의 동작 특성

- 셋업 시간(Set-up time)

* 입력 값이 플립-플롭에 안정되게 가해지기 위해서, 클럭 펄스의 트리거링이 시작되기 전에 입력 값이 유지되어야 하는 최소 시간

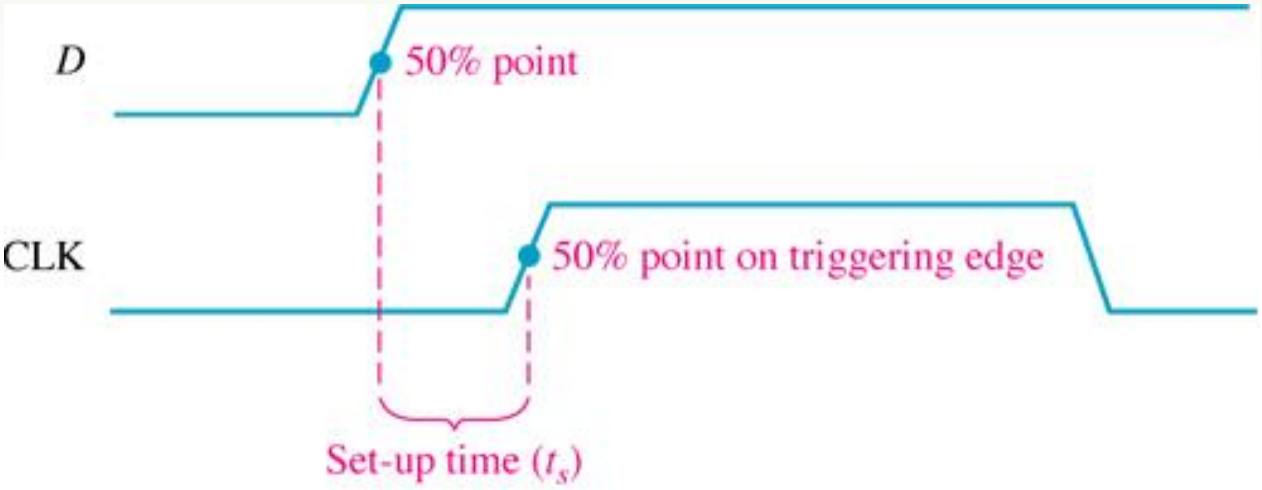


Figure 8--33 Set-up time (t_s). The logic level must be present on the D input for a time equal to or greater than t_s before the triggering edge of the clock pulse for reliable data entry.

플립-플롭의 동작 특성

- 홀드 시간(Hold time)

* 입력 값이 플립-플롭에 안정되게 가해지기 위해서, 클럭 펄스의 트리거링이 끝난 후 입력 값이 유지되어야 하는 최소 시간

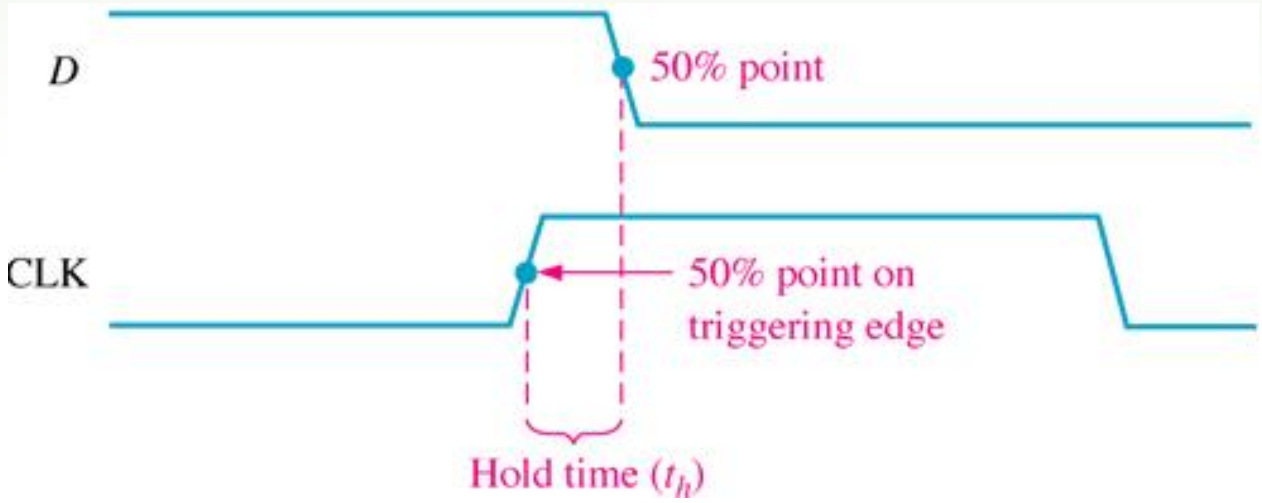


Figure 8-34 Hold time (t_h). The logic level must remain on the D input for a time equal to or greater than t_h after the triggering edge of the clock pulse for reliable data entry.

플립-플롭의 동작 특성

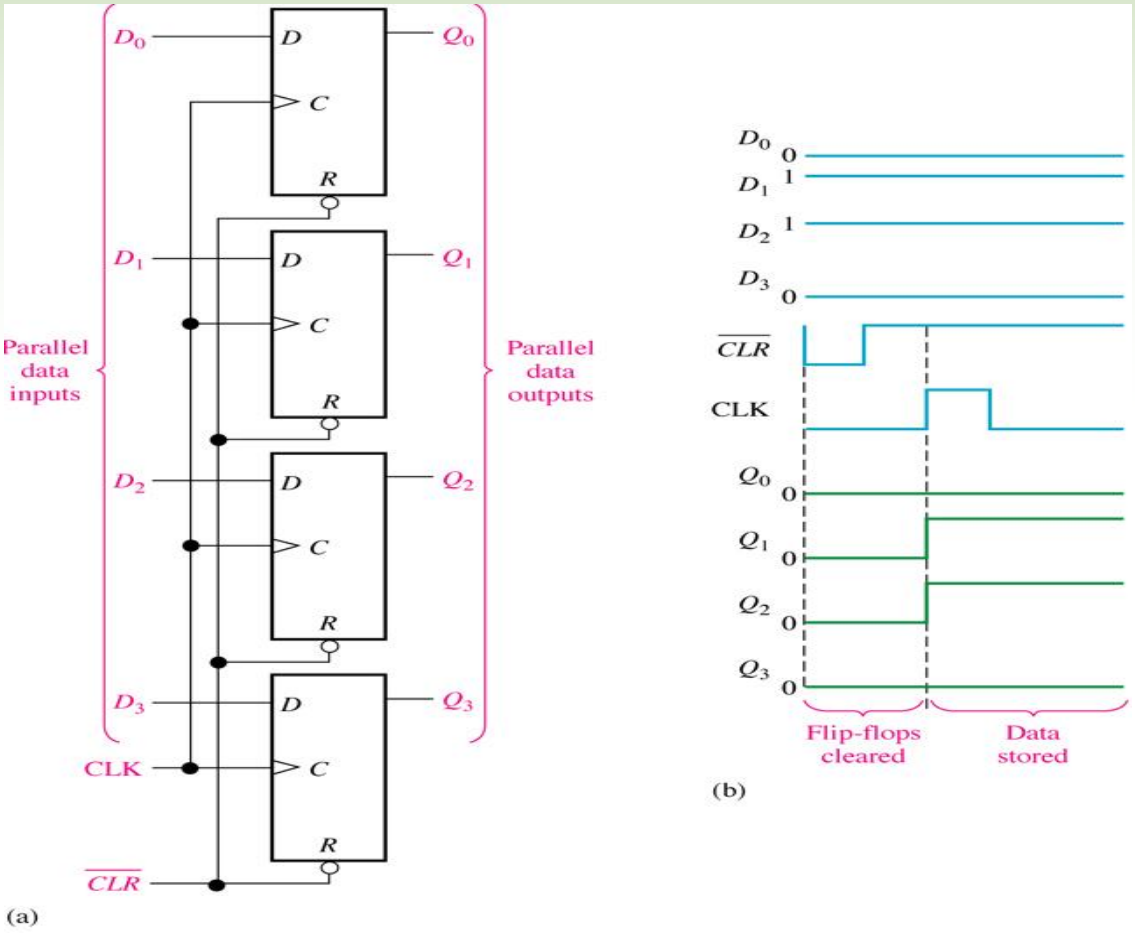
- 최대 클럭 주파수(Maximum Clock Frequency)
  * 플립-플롭이 안정되게 트리거링 될 수 있는 최고 주파수

- 펄스 폭(Pulse Widths)
  * 플립-플롭이 안정되게 동작하기 위해 필요한 clock, preset, clear 등의 최소 펄스 폭이 정의되어 있다.

- 전력 소비(Power Dissipation)
  * 소자의 전체 소비 전력

플립-플롭의 응용

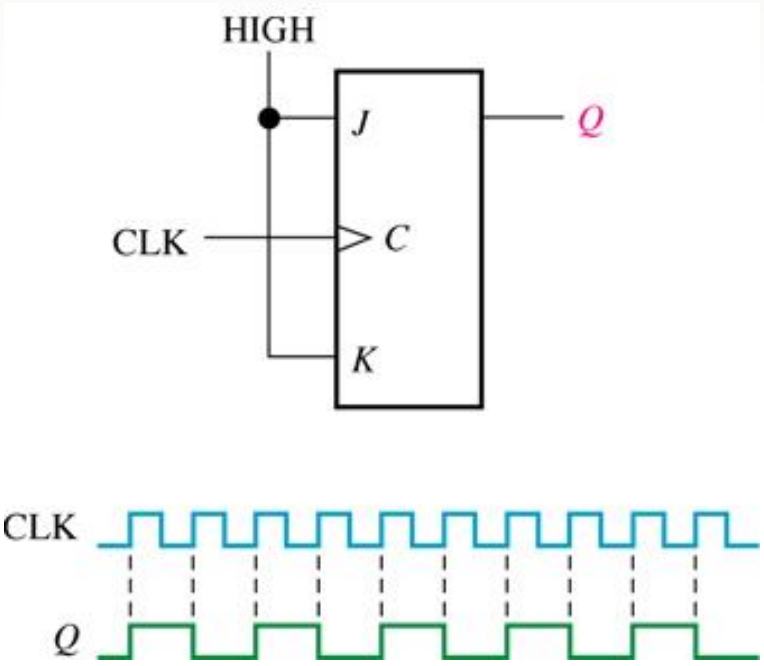
- 병렬 데이터 저장

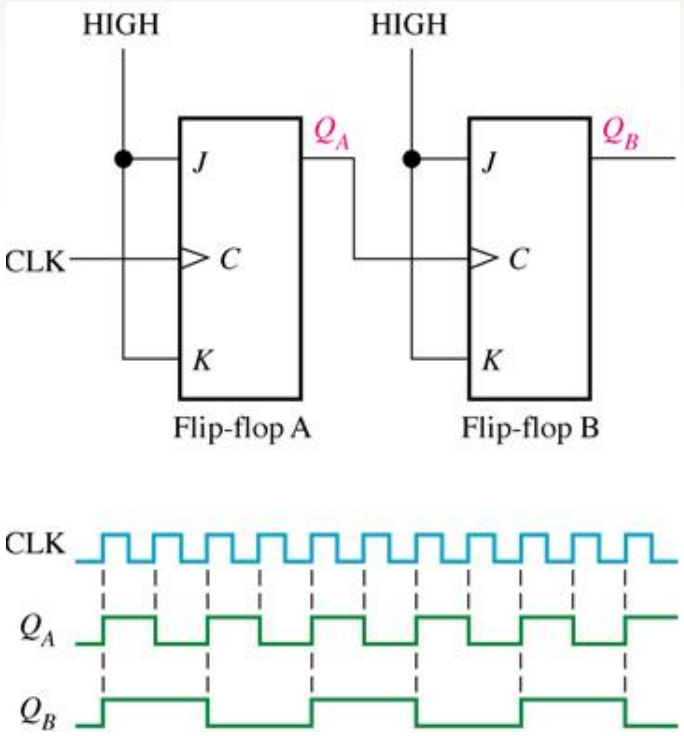


플립-플롭의 응용

- 주파수 분주

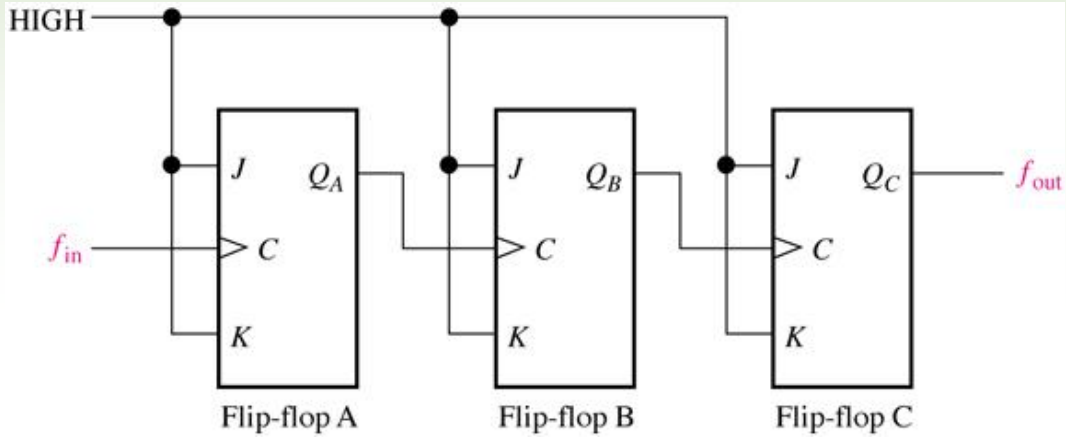
  * 주기적인 파형의 주파수를 분주할 수 있다.

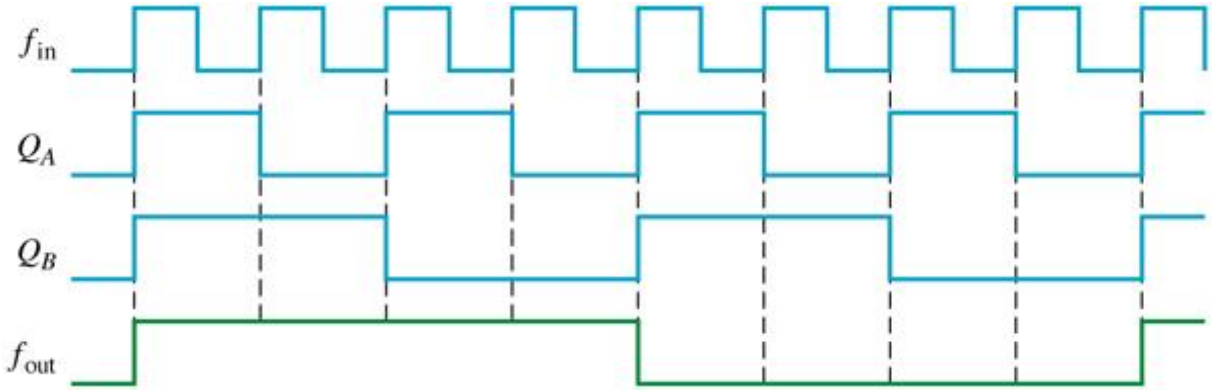




플립-플롭의 응용

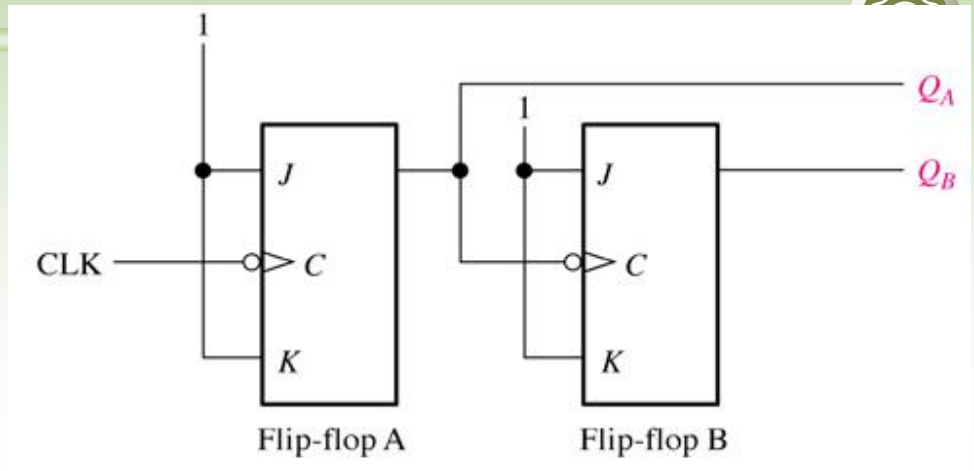
* 예제 8-11) 플립-플롭 A의 클럭 입력이 8kHz 구형파일때의 f_{out}

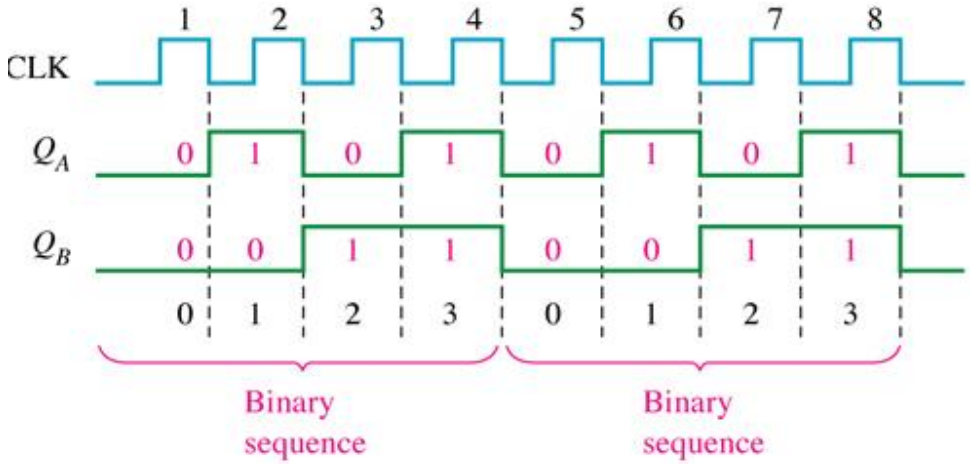




플립-플롭의 응용

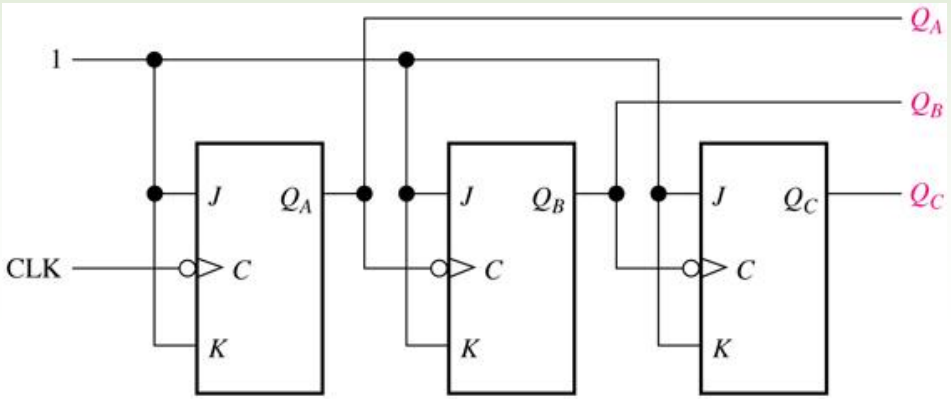
- 계수

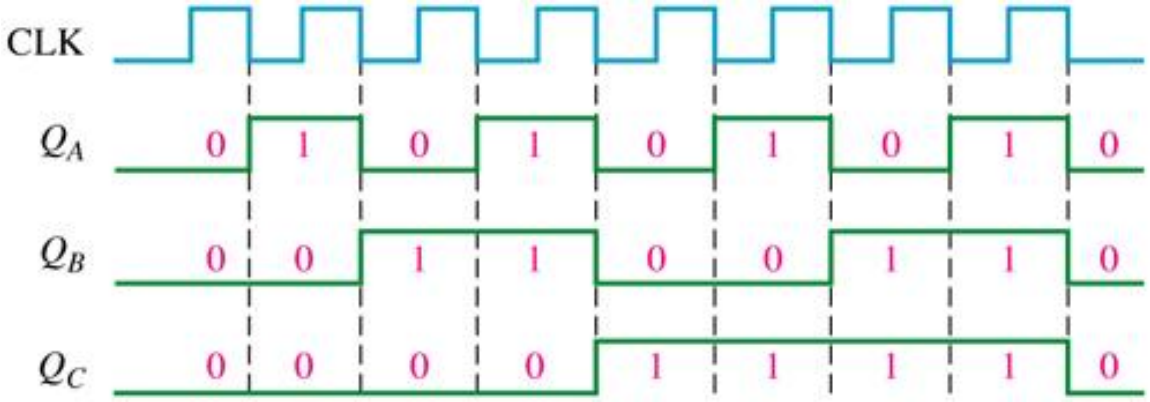

1
1
Q_A
Q_B
J
C
K
CLK
Flip-flop A
Flip-flop B


1 2 3 4 5 6 7 8
CLK
Q_A
Q_B
0 1 0 1 0 1 0 1
0 0 1 1 0 0 1 1
0 1 2 3 0 1 2 3
Binary sequence
Binary sequence

플립-플롭의 응용

* 예제 8-12)





원-샷(One-shots)

* 한 개의 안정된 상태를 갖는 단안정 멀티바이브레이터

* 트리거 입력에 대해 인버터 G2의 출력은 HIGH가되고, RC회로의 시정수에 의해 결정된 시간 동안 HIGH 유지 후 LOW로 바뀜.

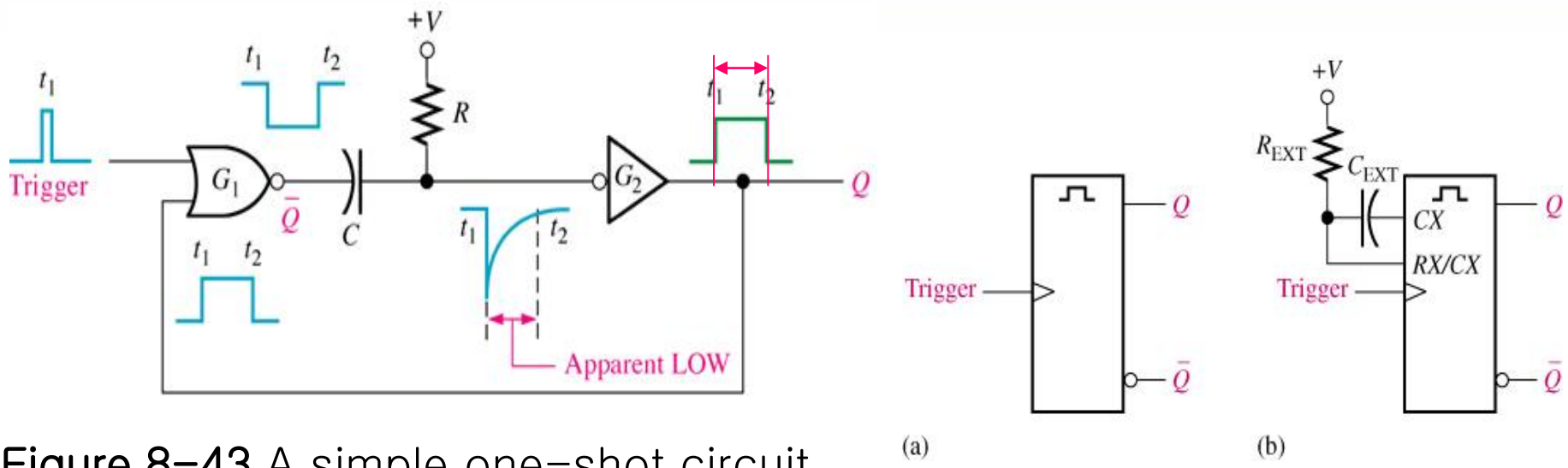
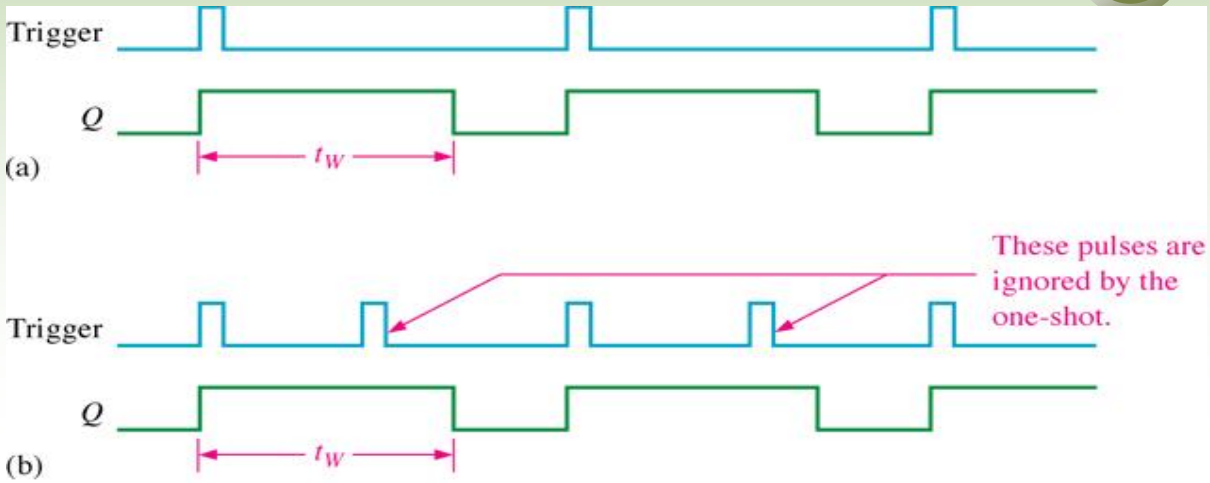


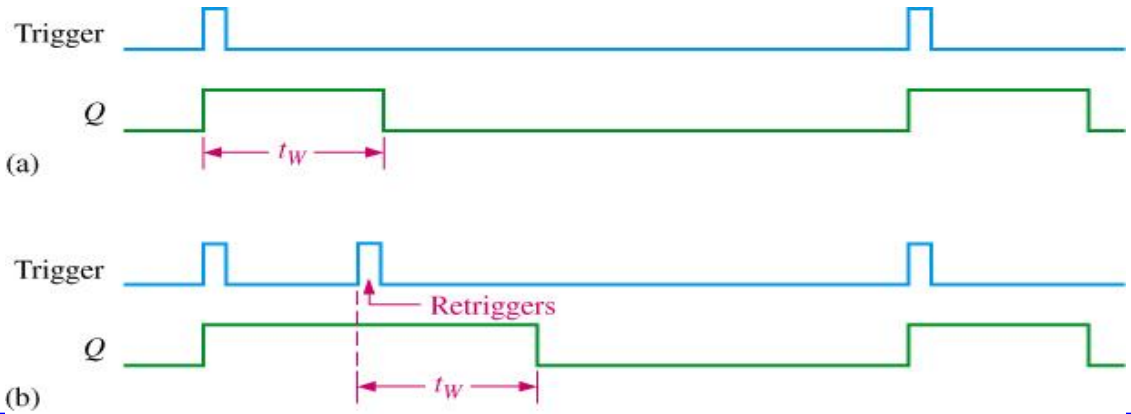
Figure 8-43 A simple one-shot circuit.

원-샷(One-shots)

* Nonretriggerable one-shot action.



* Retriggerable one-shot action.



원-샷(One-shots)

* 순차적 타이밍 회로