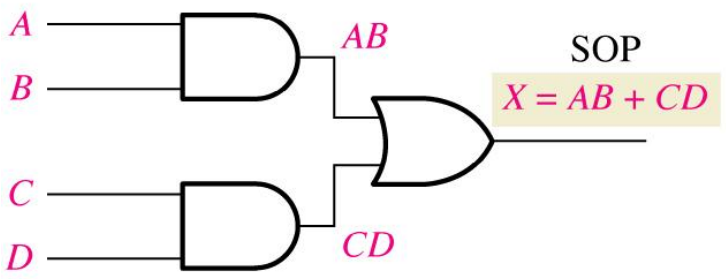
5장. 조합논리(Combinational Logic)

- 기본적인 조합 논리회로 (1)
- 조합 논리의 구현(2)
- NAND 게이트와 NOR 게이트를 이용한 조합 논리회로(3, 4)
- 펄스파형을 갖는 논리회로의 동작(5)
- (프로그래머블 논리 : CPLD(7))

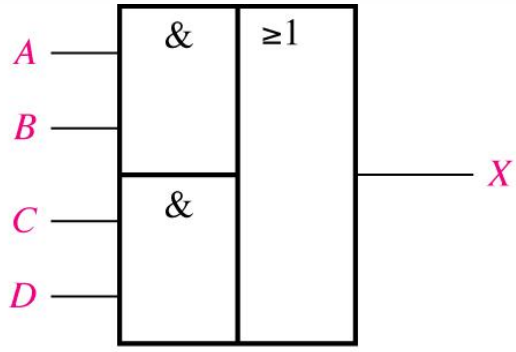
기본적인 조합 논리회로

- 조합 논리(Combinational Logic)

- AND-OR 논리



(a) Logic diagram (ANSI standard distinctive shape symbols)



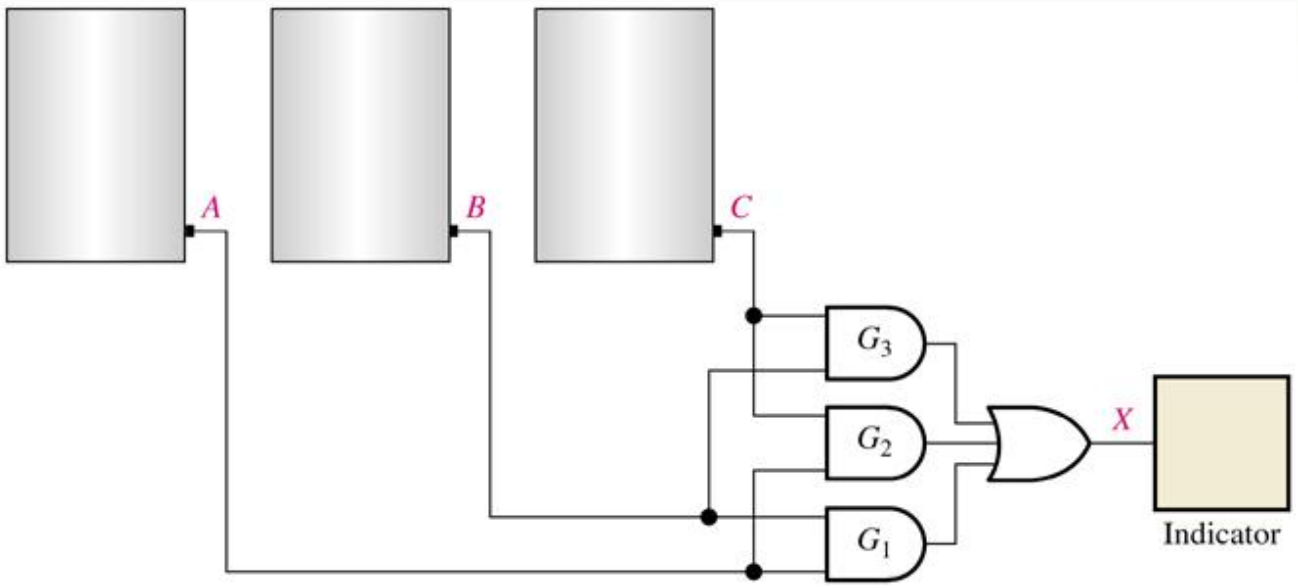
(b) ANSI standard rectangular outline symbol

* A와 B가 모두 1이거나, C와 D가 모두 1인 경우에 출력 X가 1이 된다.

기본적인 조합 논리회로

(예제 5-1) 화학물의 양이 특정 지점 이하로 떨어지면 센서가 HIGH 출력.
임의의 두 저장고의 화학물의 양이 특정 지점 이하로 떨어지는 경우를 검출.

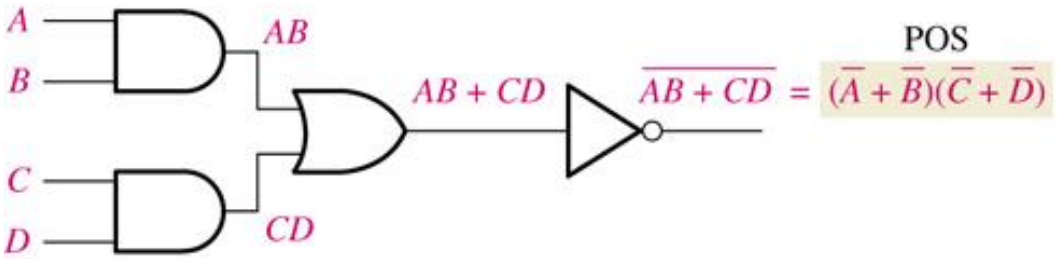
=> X=AB+BC+AC

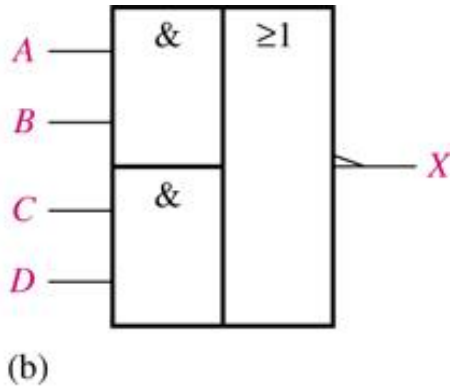


기본적인 조합 논리회로

- AND-OR-인버터 논리

* (A'+B')(C'+D')=(AB)'(CD)'= ((AB)'(CD)')"=((AB)"+(CD)")'=(AB+CD)'



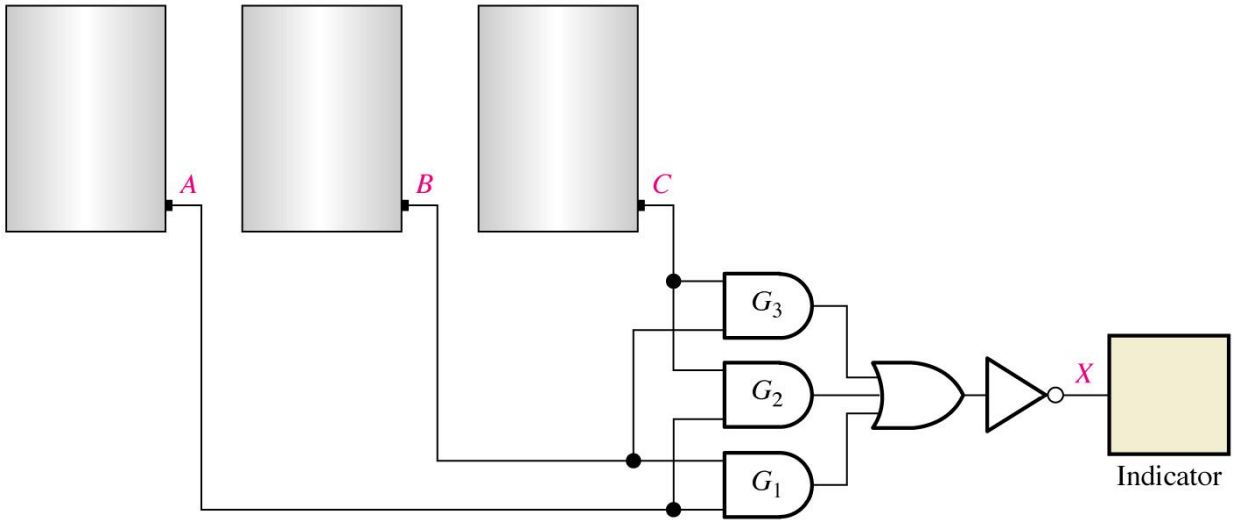


* A와 B가 모두 1이거나, C와 D가 모두 1인 경우에 출력 X가 0이 된다.

기본적인 조합 논리회로

(예제 5-2) 화학물의 양이 특정 지점 이하로 떨어지면 센서가 LOW 출력.
임의의 두 저장고의 화학물의 양이 특정 지점 이하로 떨어지는 경우를 검출.

=> X=(AB+BC+AC)′=(A′+B′)(B′+C′)(A′+C′)

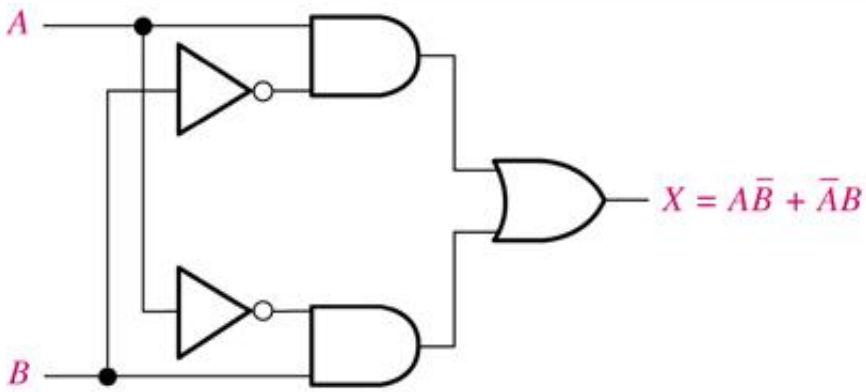


기본적인 조합 논리회로

- 배타적-OR 논리 ; X=AB'+A'B = A ⊕ B

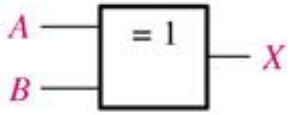
Truth Table

Input A	Input B	Output X
0	0	0
0	1	1
1	0	1
1	1	0



(a) Logic diagram

(b) ANSI distinctive shape symbol



(c) ANSI rectangular outline symbol

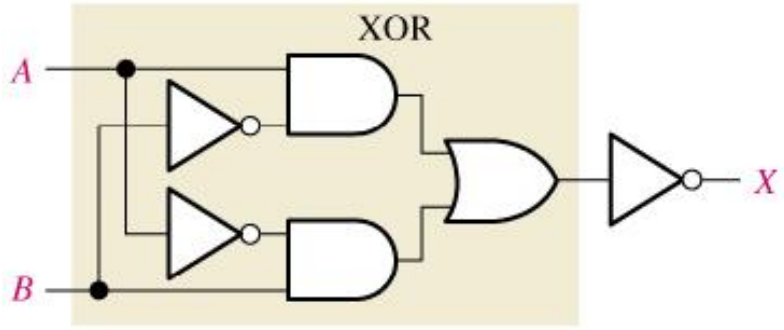
기본적인 조합 논리회로

- 배타적-NOR 논리 ;

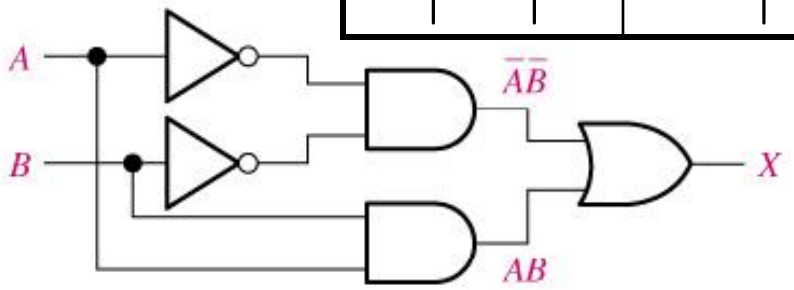
$X=(AB'+A'B)' = (AB')'(A'B)'=(A'+B)(A+B')=A'B'+AB$

Truth Table

Input A	Input B	Output X
0	0	1
0	1	0
1	0	0
1	1	1



(a) $X = A\overline{B} + \overline{A}B$

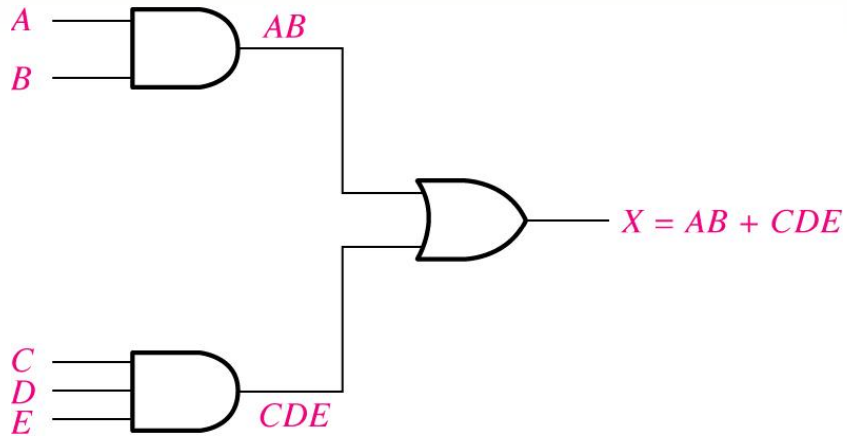


(b) $X = \overline{A}\overline{B} + AB$

조합 논리의 구현

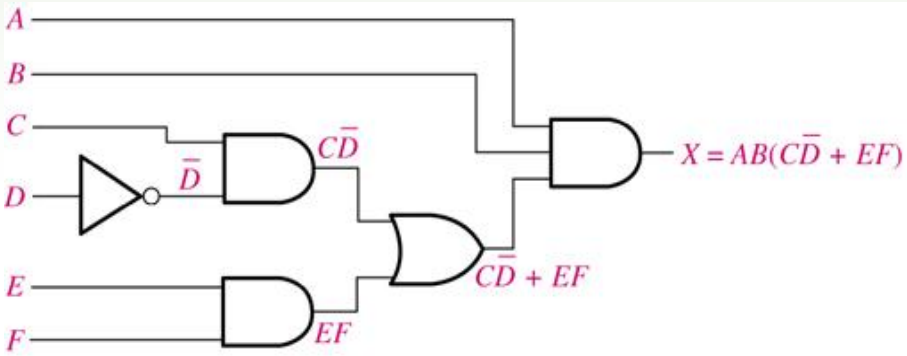
- 부울식으로부터 논리회로 유도
  - * 부울 식 ⇔ 논리회로

X=AB+CDE

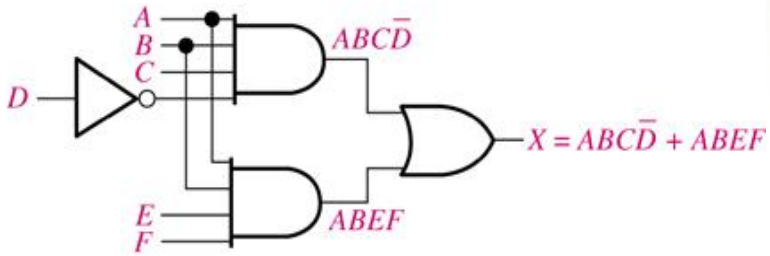


조합 논리의 구현

* 부울 식 ⇔ 논리회로



(a)



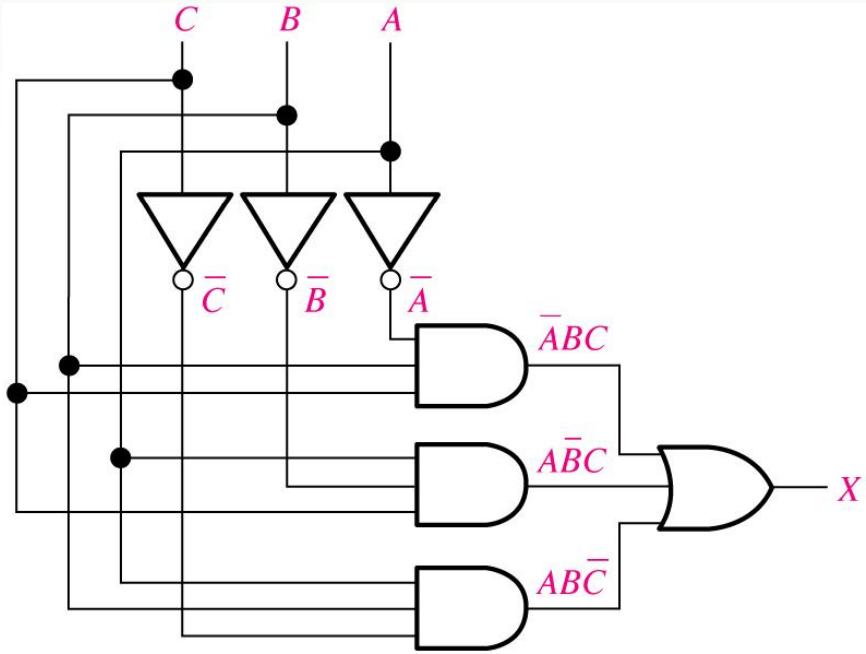
(b) Sum-of-products implementation of the circuit in part (a)

조합 논리의 구현

- 진리표로부터 논리회로 유도
  - * 진리표 ⇔ 논리회로

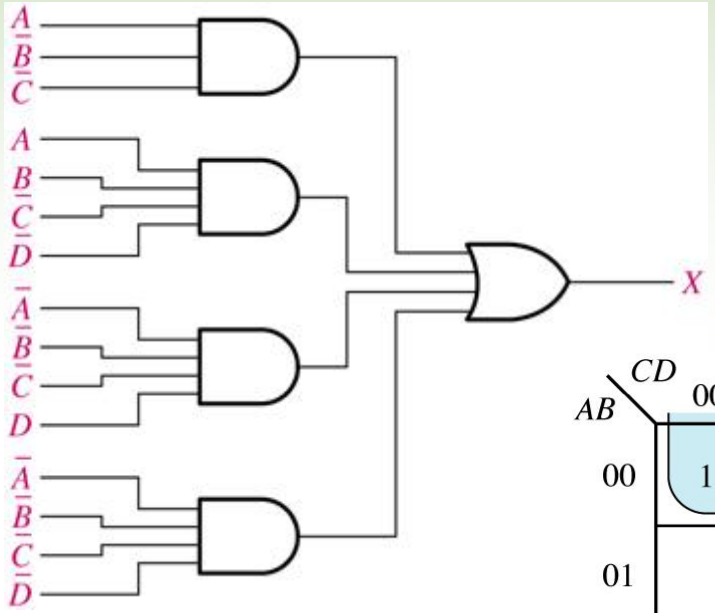
예제 5-3) 진리표의 연산을 충족시키는 논리회로를 설계하라.

Inputs A	B	C	Output X	Product Term
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	1	A'BC
1	0	0	0	
1	0	1	1	AB'C
1	1	0	1	ABC'
1	1	1	0	



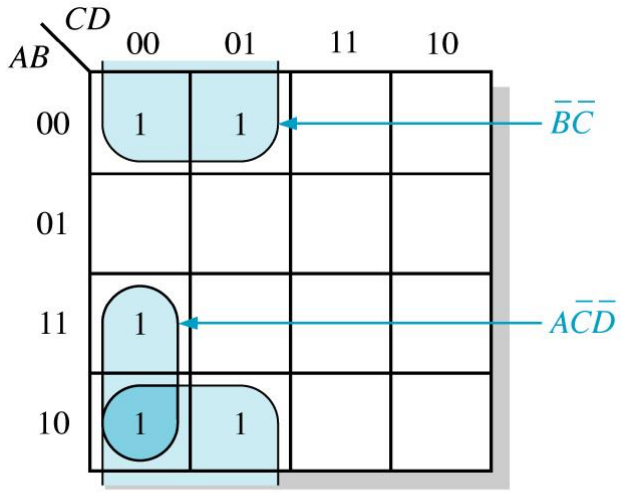
조합 논리의 구현

예제 5-6) 다음 조합 논리회로를 최소화하라.

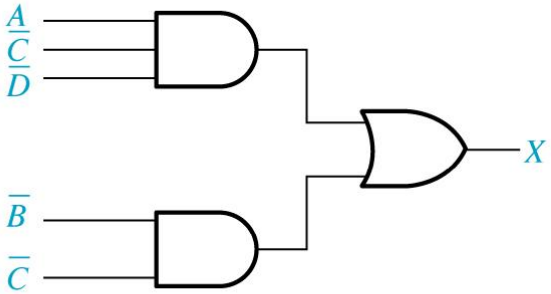


=> X= AB'C'+ABC'D'+A'B'C'D+A'B'C'D'

=> X= AB'C'D+AB'C'D'
+ABC'D'+A'B'C'D+A'B'C'D'



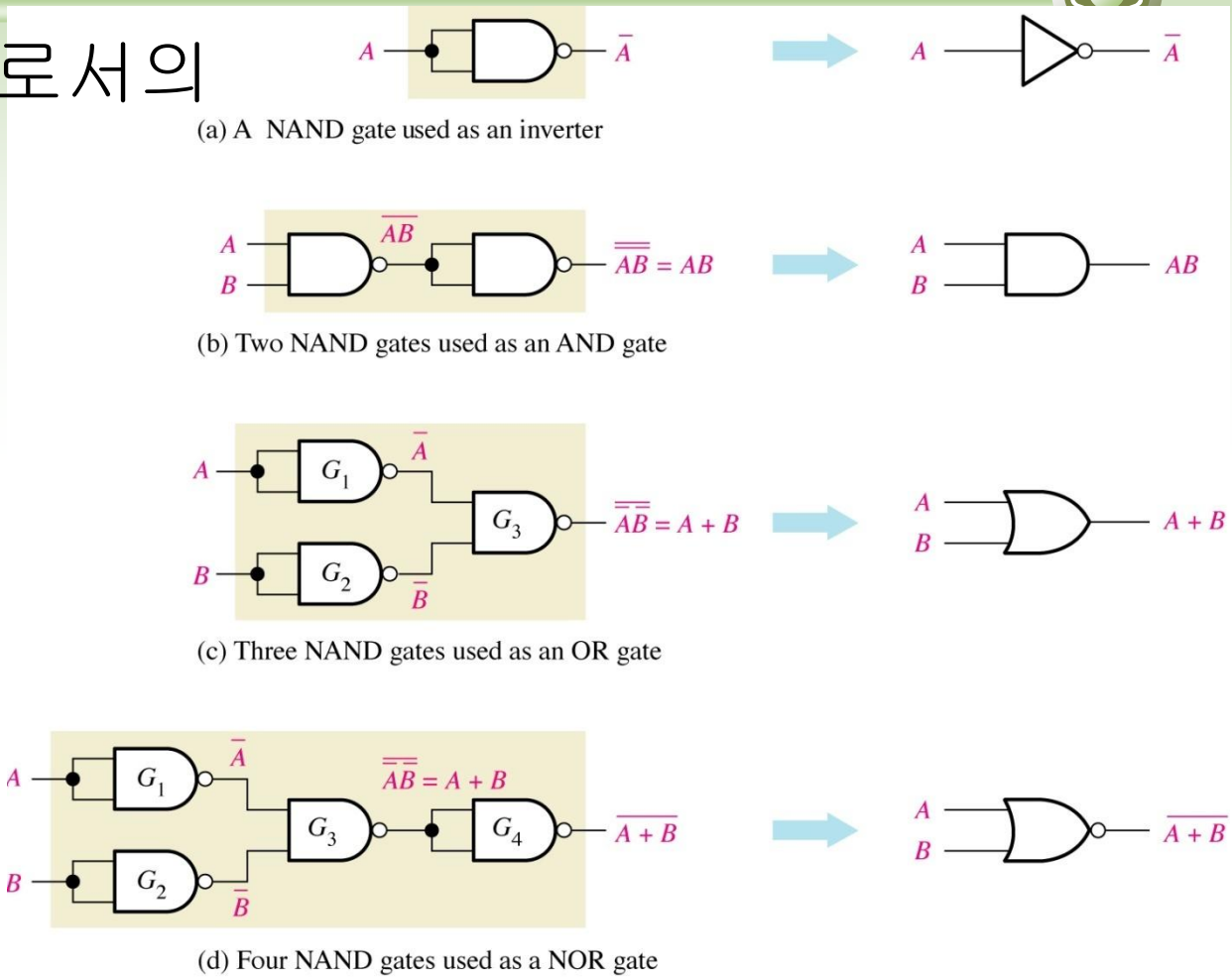
(a)



(b)

NAND 게이트와 NOR게이트의 만능 특성

- 만능 논리 요소로서의 NAND 게이트

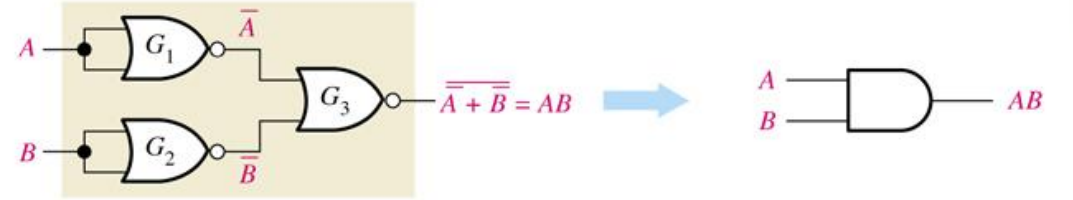


NAND 게이트와 NOR게이트의 만능 특성

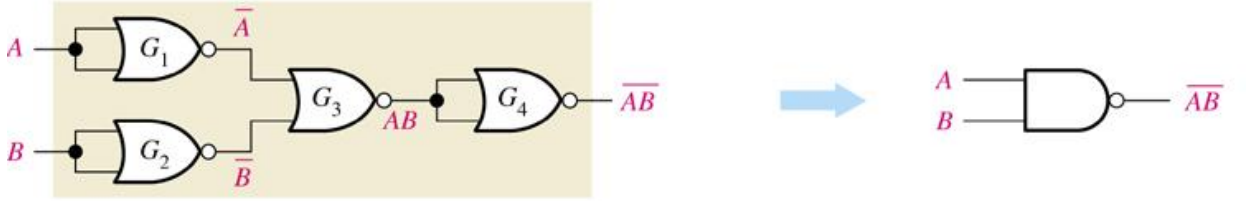
- 만능 논리 요소로서의 NOR 게이트

(a) A NOR gate used as an inverter

(b) Two NOR gates used as an OR gate



(c) Three NOR gates used as an AND gate



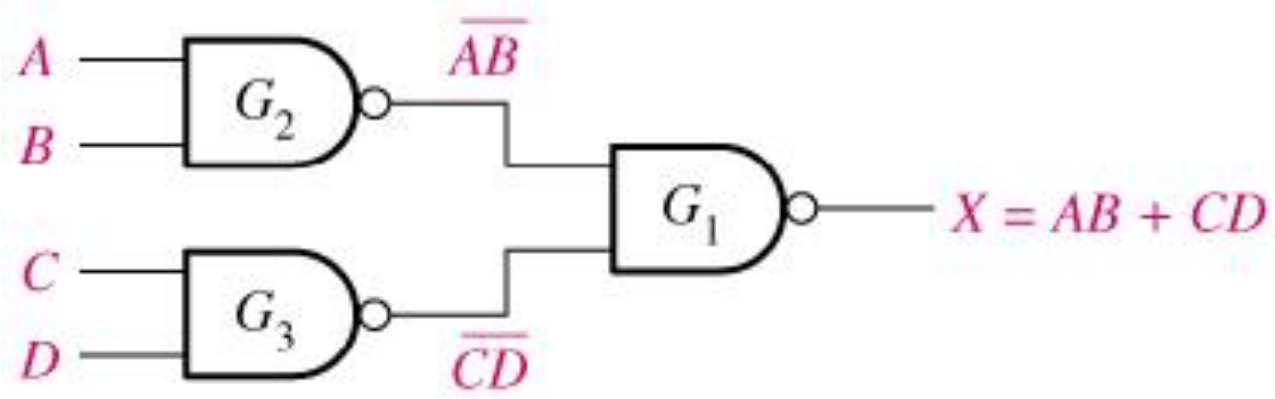
(d) Four NOR gates used as a NAND gate

NAND 게이트와 NOR게이트를 이용한 조합 회로

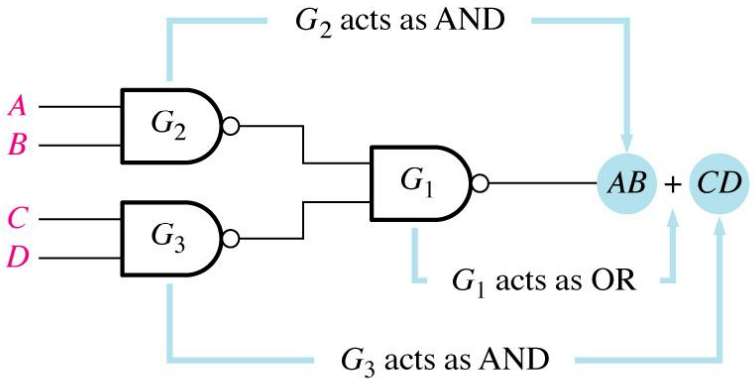
- NAND 논리

* NAND = 부 OR; (AB)′ =

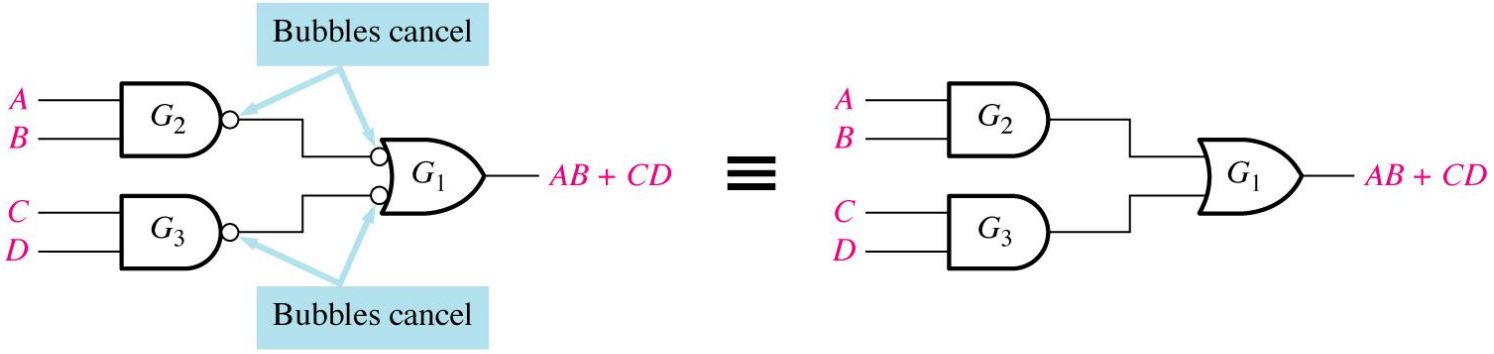
* X = ((AB)′(CD)′)′ = AB + CD



NAND 게이트와 NOR게이트를 이용한 조합 회로



(a) Original NAND logic diagram showing effective gate operation relative to the output expression



(b) Equivalent NAND/Negative-OR logic diagram

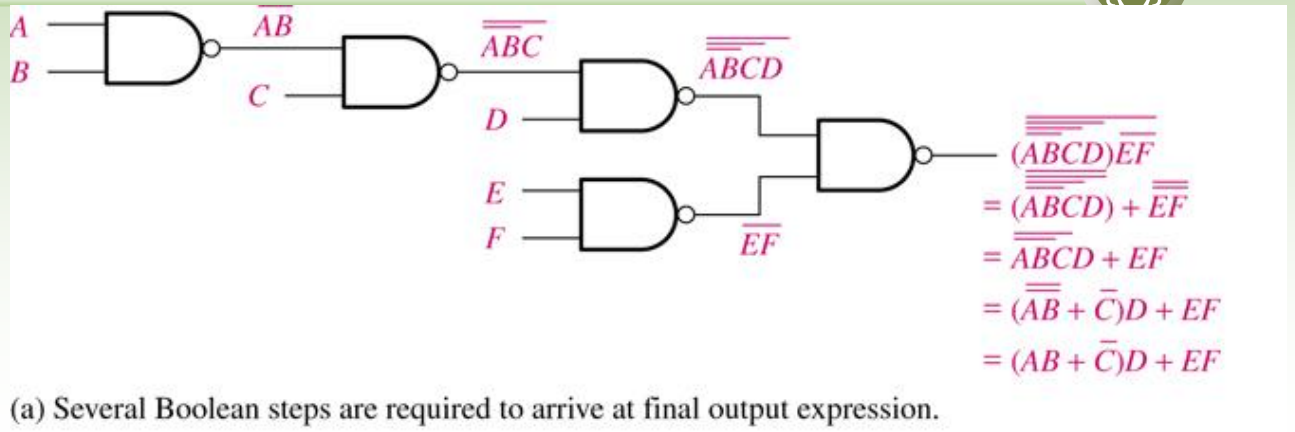
(c) AND-OR equivalent

NAND 게이트와 NOR게이트를 이용한 조합 회로

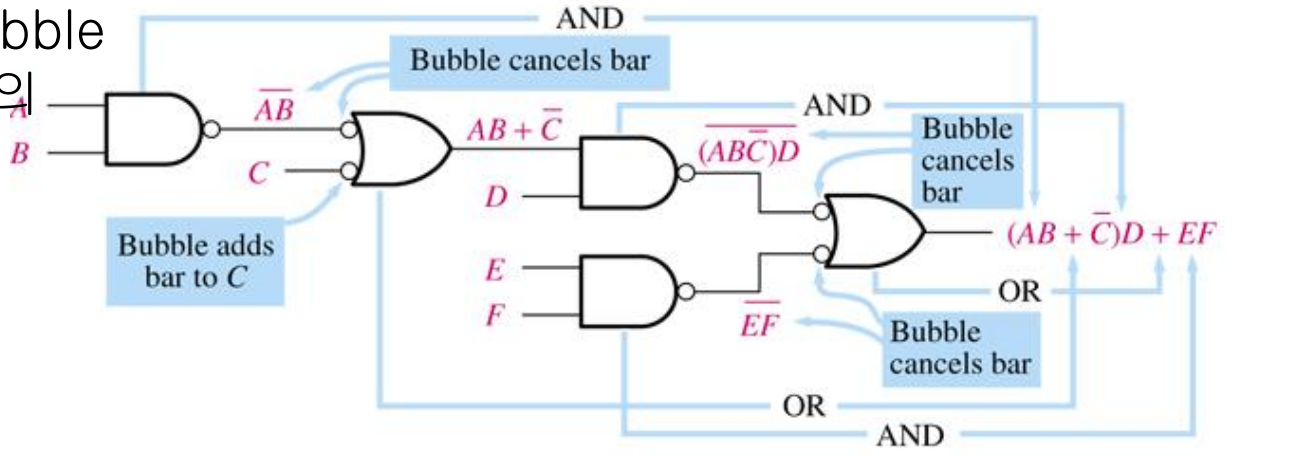
- NAND 논리도

* NAND 또는 부-OR 기호를 사용

* bubble-to-bubble 또는 Nonbubble-to-nonbubble 로 표시하는 것이 회로의 해석에 편리.



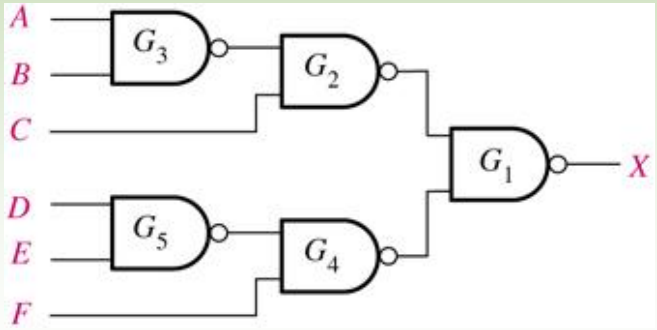
(a) Several Boolean steps are required to arrive at final output expression.

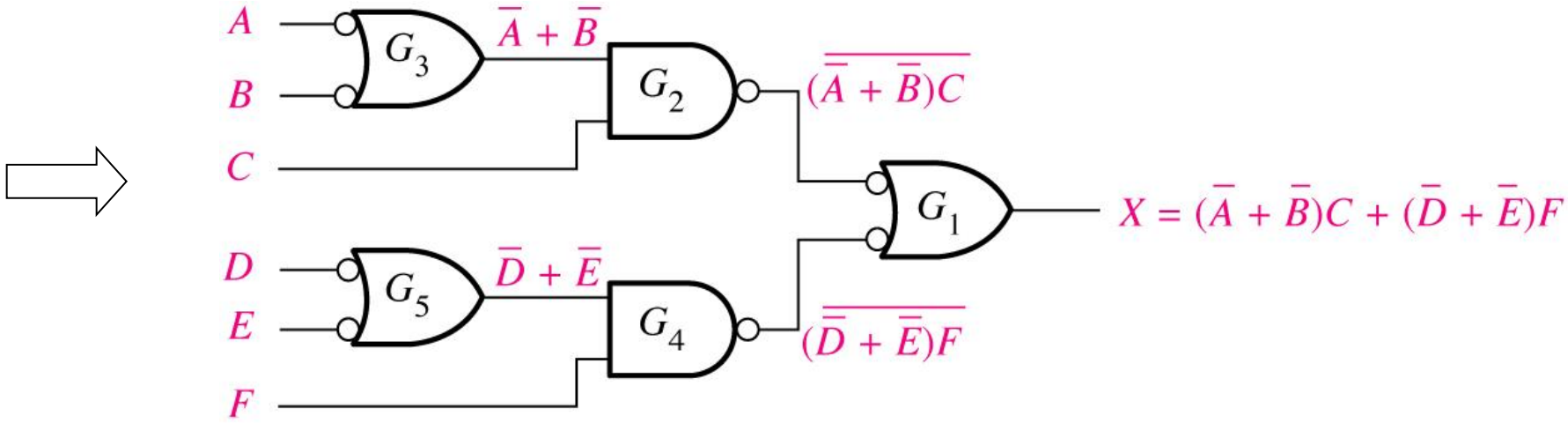


(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

NAND 게이트와 NOR게이트를 이용한 조합 회로

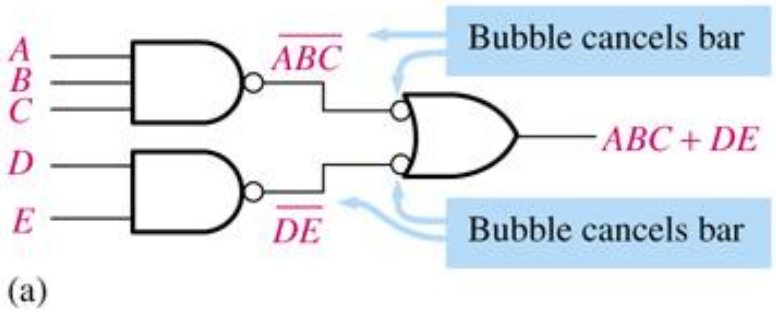
* 예제 5-7)

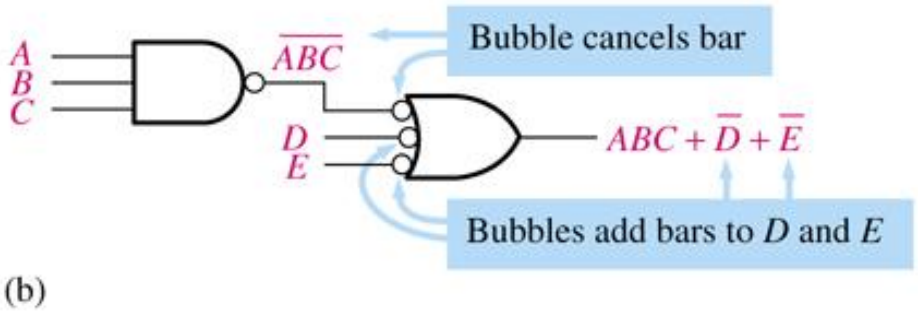




NAND 게이트와 NOR게이트를 이용한 조합 회로

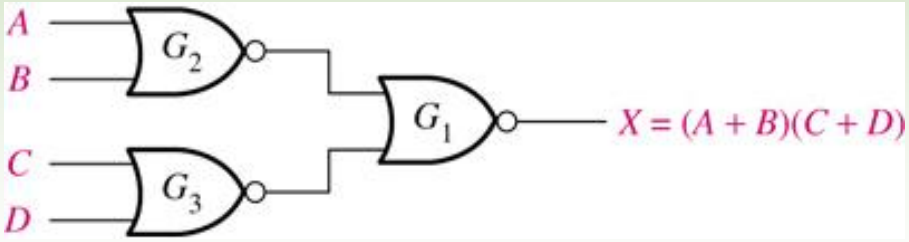
* 예제 5-8) ABC+DE, ABC+D'+E' 를 NAND 논리를 이용하여 구현하라.

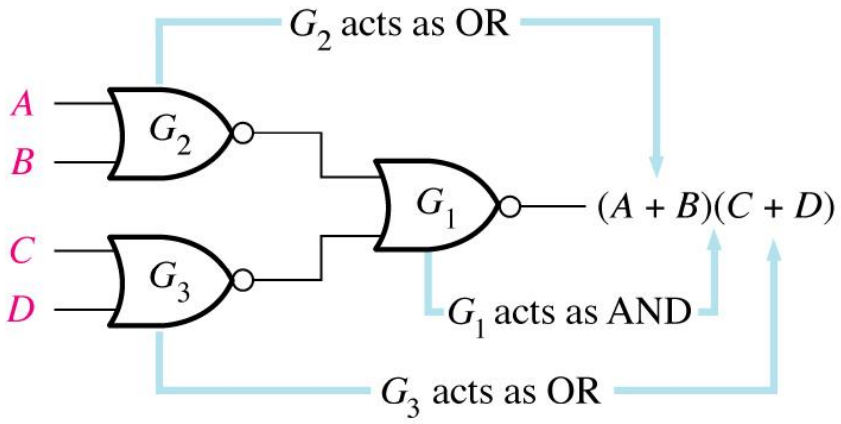




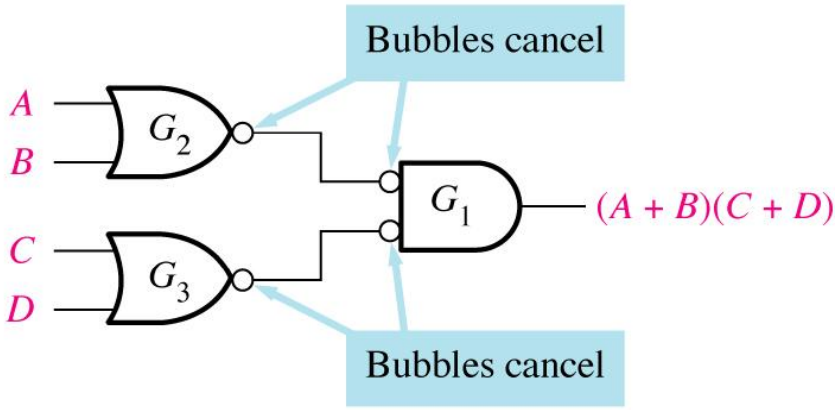
NAND 게이트와 NOR게이트를 이용한 조합 회로

- NOR 논리
  - * NOR = 부 AND; (A+B)′ = A′ B′
  - * X = ((A+B)′+(C+D)′)′ = (A+B)(C+D)





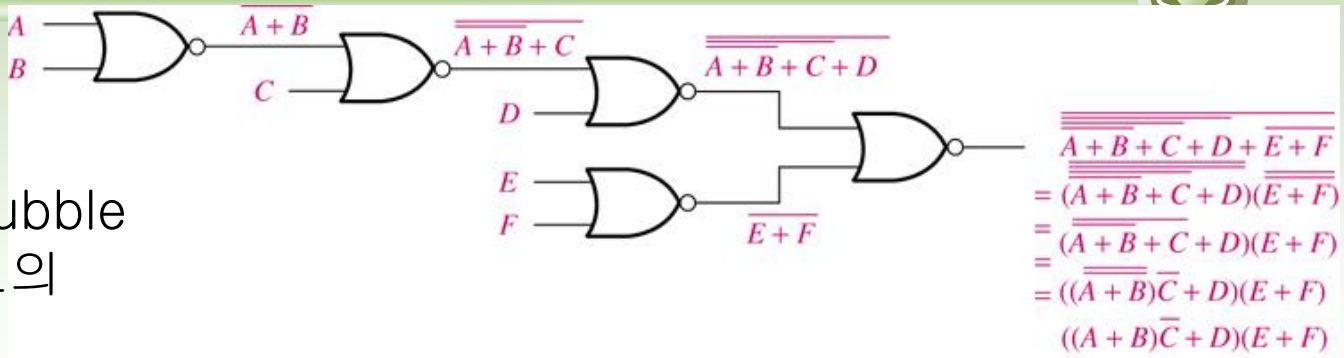
(a)



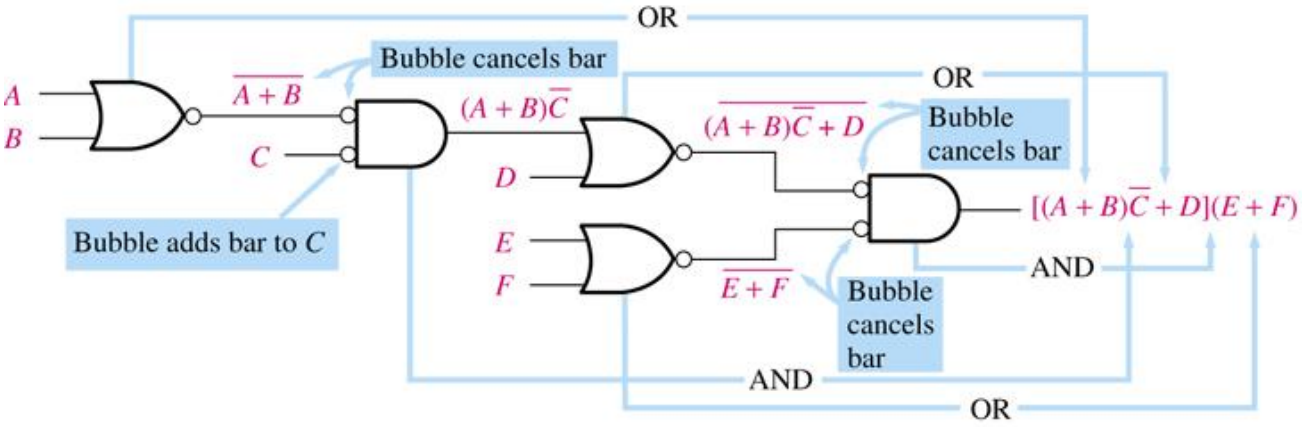
(b)

NAND 게이트와 NOR게이트를 이용한 조합 회로

* bubble-to-bubble 또는 Nonbubble-to-nonbubble 로 표시하는 것이 회로의 해석에 편리.



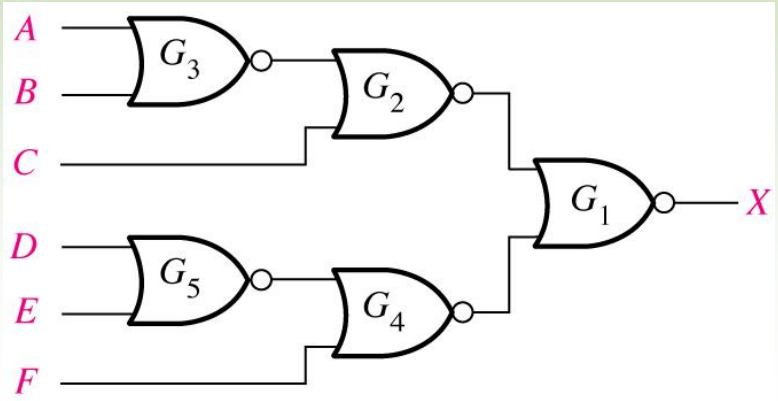
(a) Final output expression is obtained after several Boolean steps.

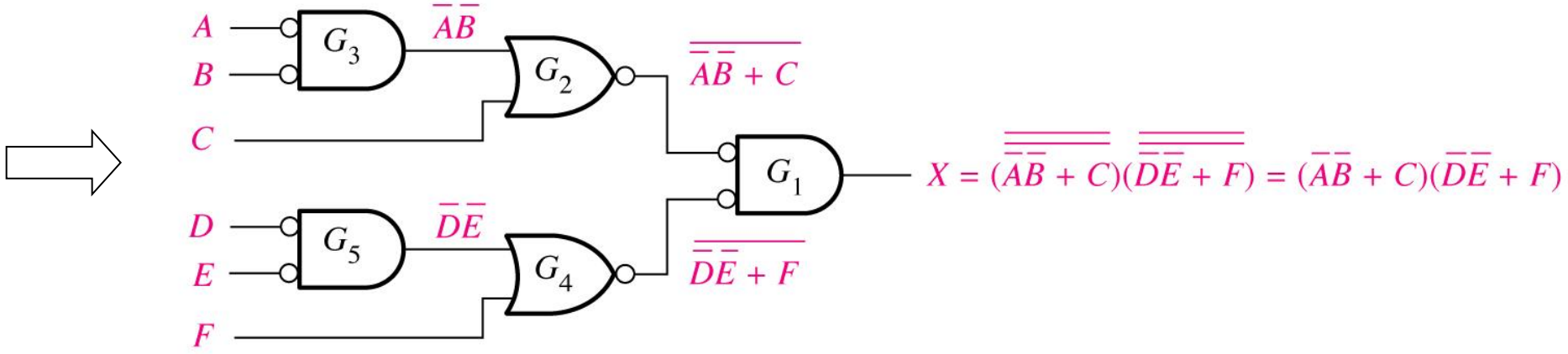


(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

NAND 게이트와 NOR게이트를 이용한 조합 회로

* 예제 5-9)

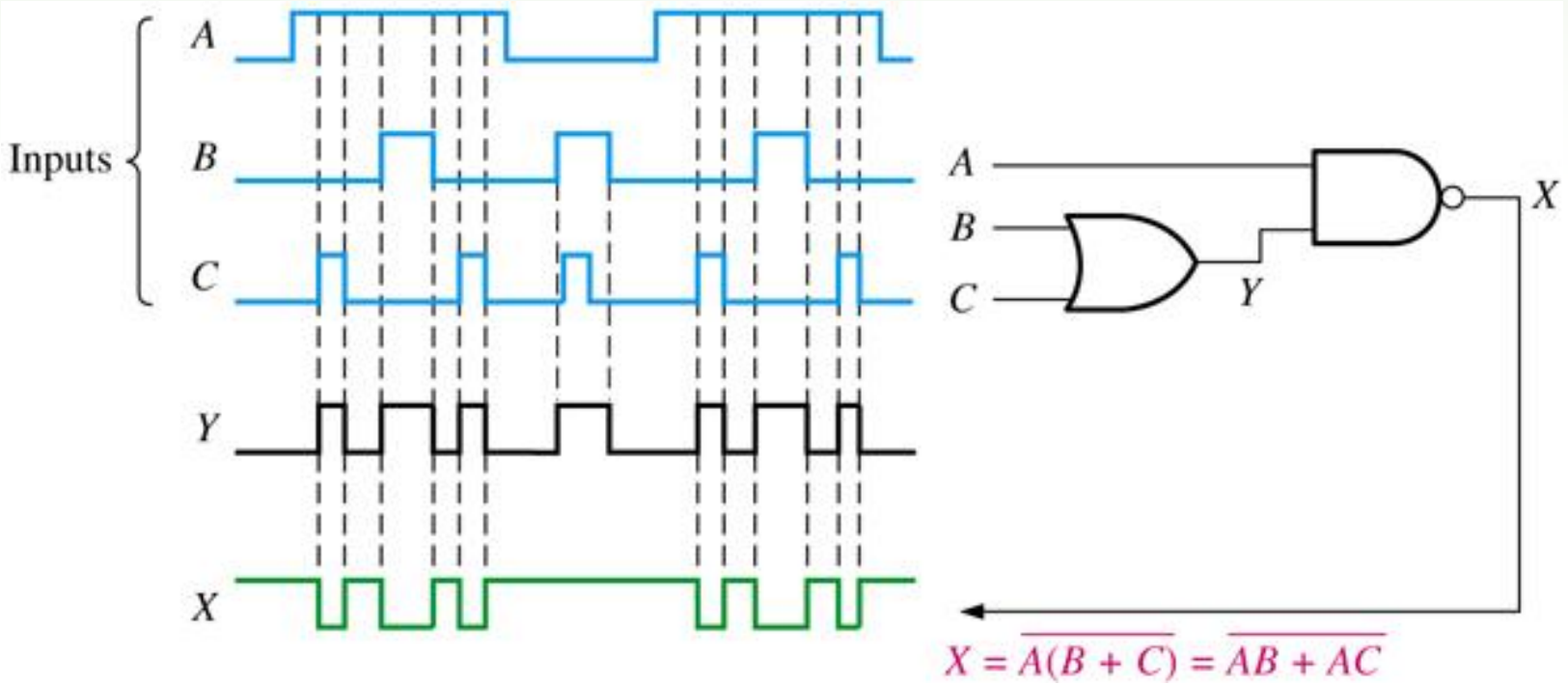




펄스 파형을 갖는 논리회로 동작

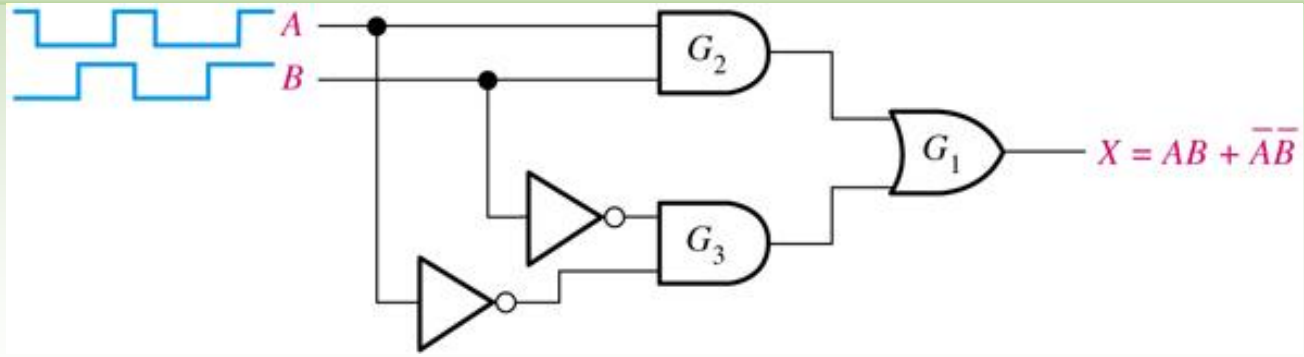
* 게이트의 동작은 입력이 펄스이던, 시불변이던 같다.

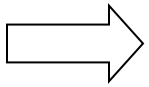
* 예제 5-10) 입력파형 A, B, C에 따른 출력 X의 파형.

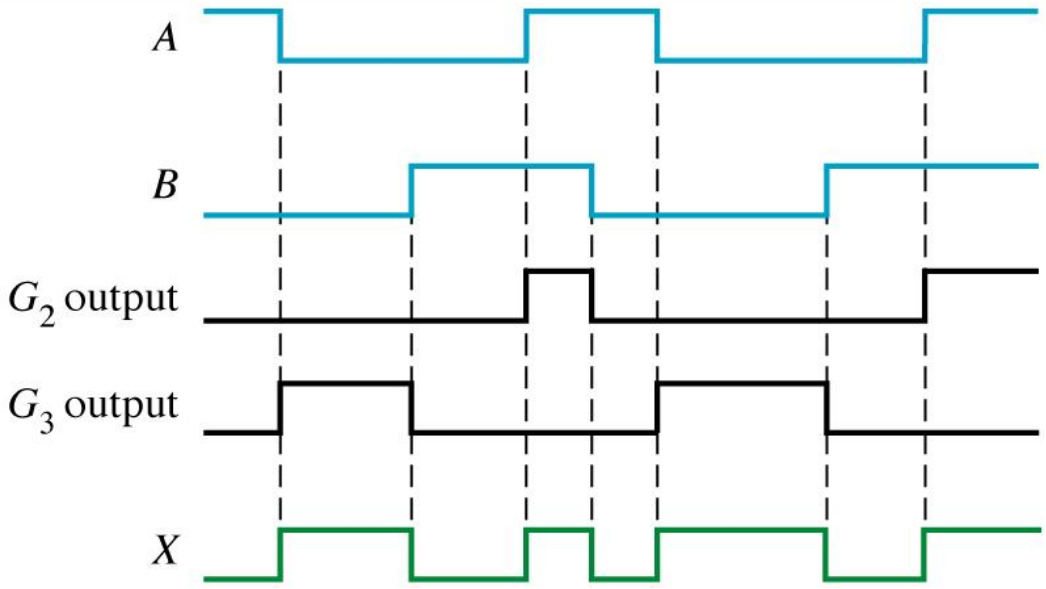


펄스 파형을 갖는 논리회로 동작

* 예제 5-11)

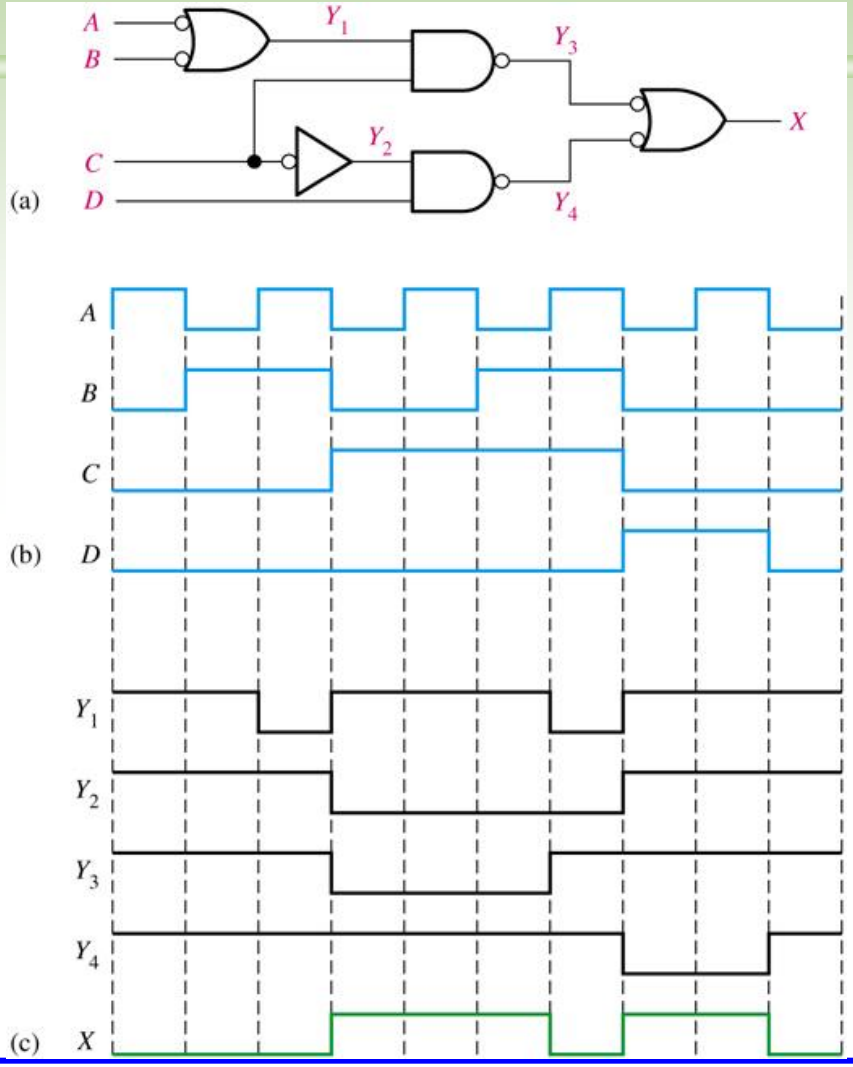






펄스 파형을 갖는 논리회로 동작

* 예제 5-12)



펄스 파형을 갖는 논리회로 동작

* 예제 5-13) 예제5-12의 출력식으로부터 직접 출력 파형 X를 구하라.