

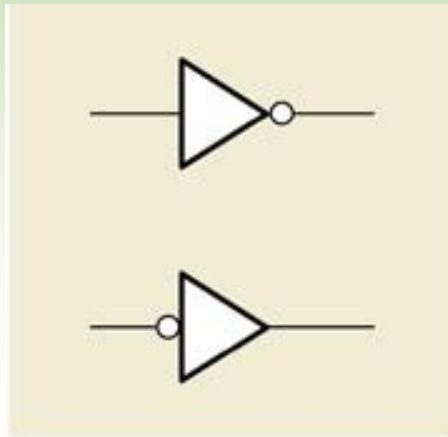
3장. 논리 게이트(Logic Gates)



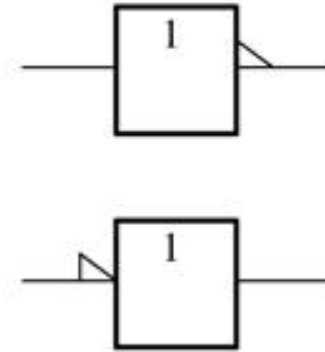
- 인버터 (1)
- AND 게이트(2)
- OR 게이트(3)
- NAND 게이트(4)
- NOR 게이트(5)
- 배타적-OR, 배타적-NOR(6)
- 고정-기능 논리:IC 게이트(7)

인버터 (Inverter)

- 표준 논리 기호



(a) Distinctive shape symbols with negation indicators



(b) Rectangular outline symbols with polarity indicators

- 인버터 진리표

인버터 (Inverter)



인버터 연산

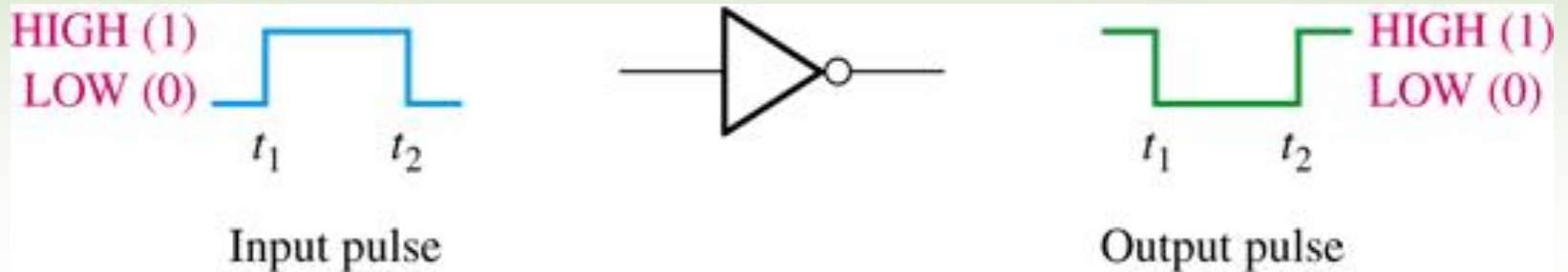


Figure 3--2 Inverter operation with a pulse input.

인버터 타이밍 도

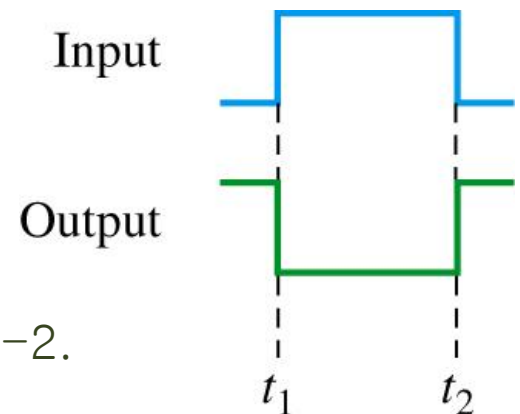
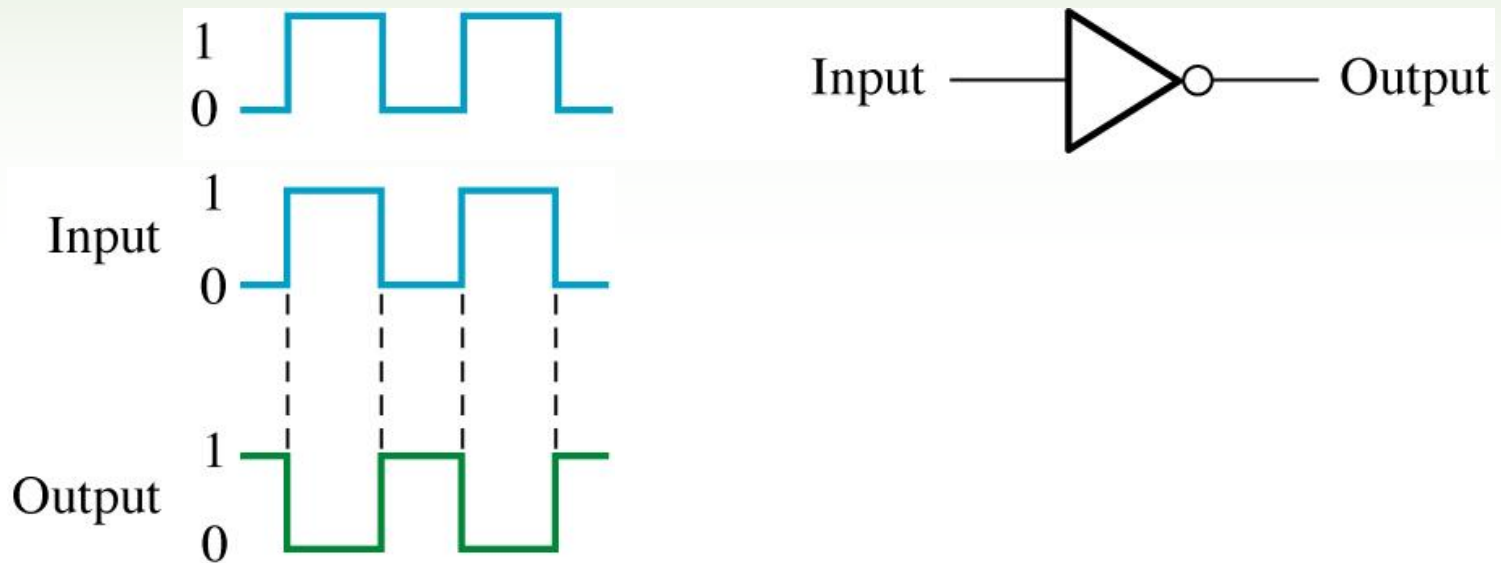


Figure 3-3 Timing diagram for the case in Figure 3-2.

인버터 (Inverter)

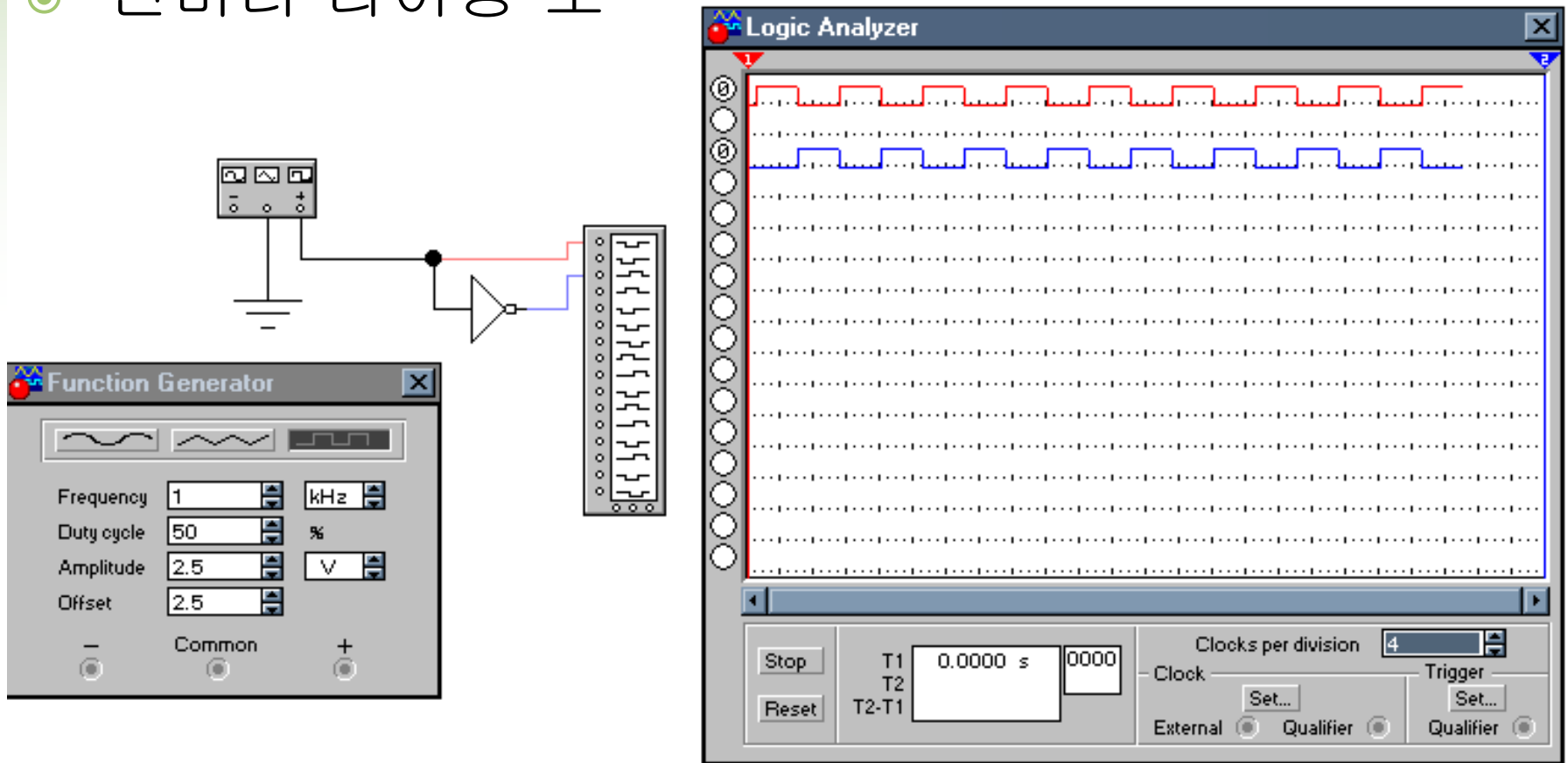


예제 3-1) 출력 파형 및 타이밍도를 구하라.



인버터 (Inverter)

인버터 타이밍 도



인버터 (Inverter)



- 인버터에 대한 논리식;

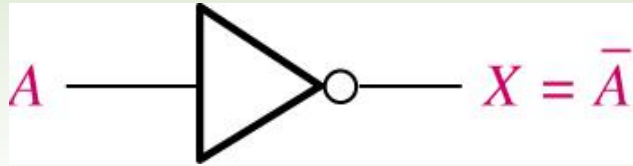


Figure 3-6 The inverter complements an input variable.

- 응용 예;

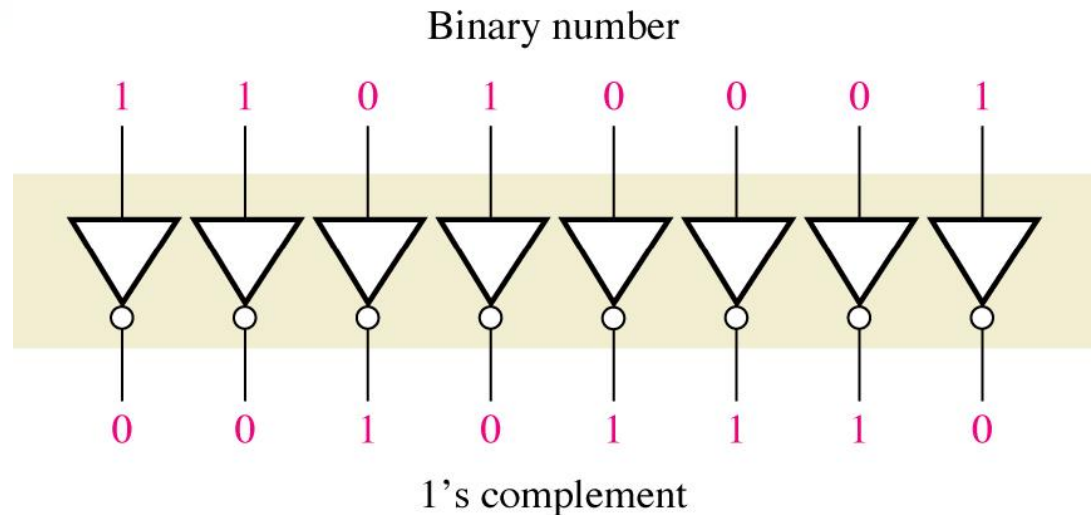
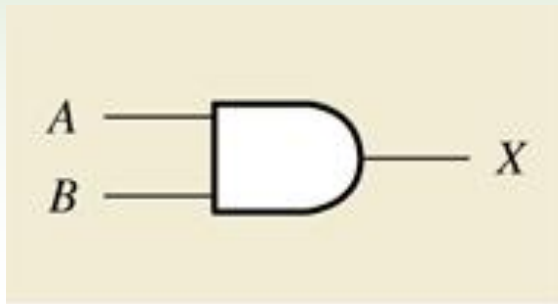


Figure 3-7 Example of a 1's complement circuit using inverters.

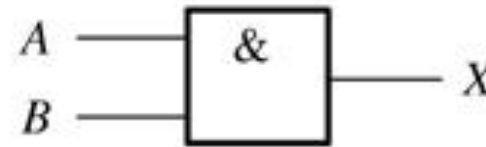
AND 게이트(AND Gate)



표준 논리 기호



(a) Distinctive shape



(b) Rectangular outline
with the AND (&
qualifying symbol

Figure 3–8 Standard logic symbols for the AND gate showing two inputs (A NSI/IEEE Std. 91–1984).

AND 게이트(AND Gate)



AND 게이트의 연산



Figure 3-9 All possible logic levels for a 2-input AND gate. Open file F 03-09 to verify the AND gate operation.

AND 게이트(AND Gate)



AND 게이트의 진리표

Input A	Input B	Output X
Low (0)	Low (0)	Low (0)
Low (0)	High (1)	Low (0)
High (1)	Low (0)	Low (0)
High (1)	High (1)	High (1)

AND 게이트(AND Gate)

AND 게이트의 펄스 연산

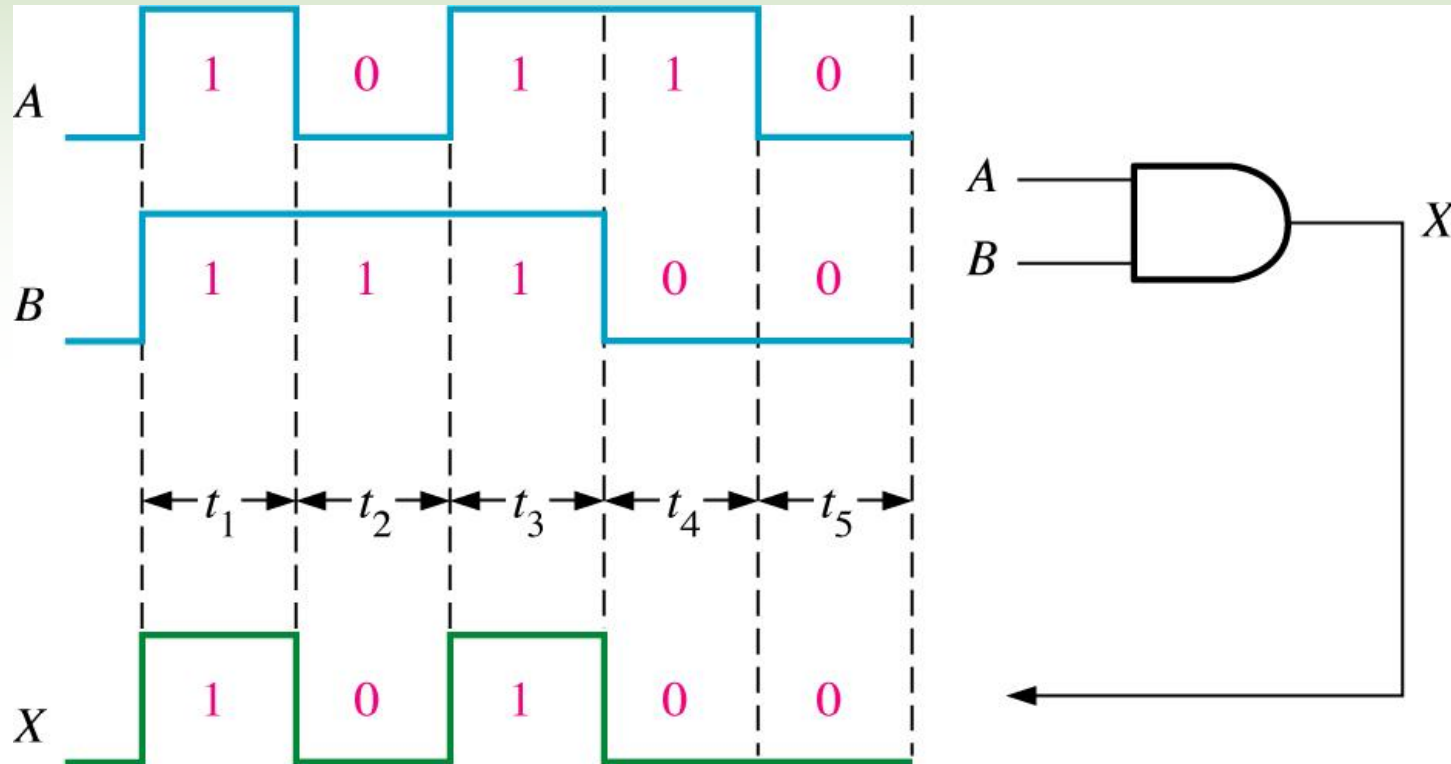


Figure 3-10 Example of pulsed AND gate operation with a timing diagram showing input and output relationships.

Inputs

A HIGH LOW

B HIGH LOW

Output X HIGH LOW

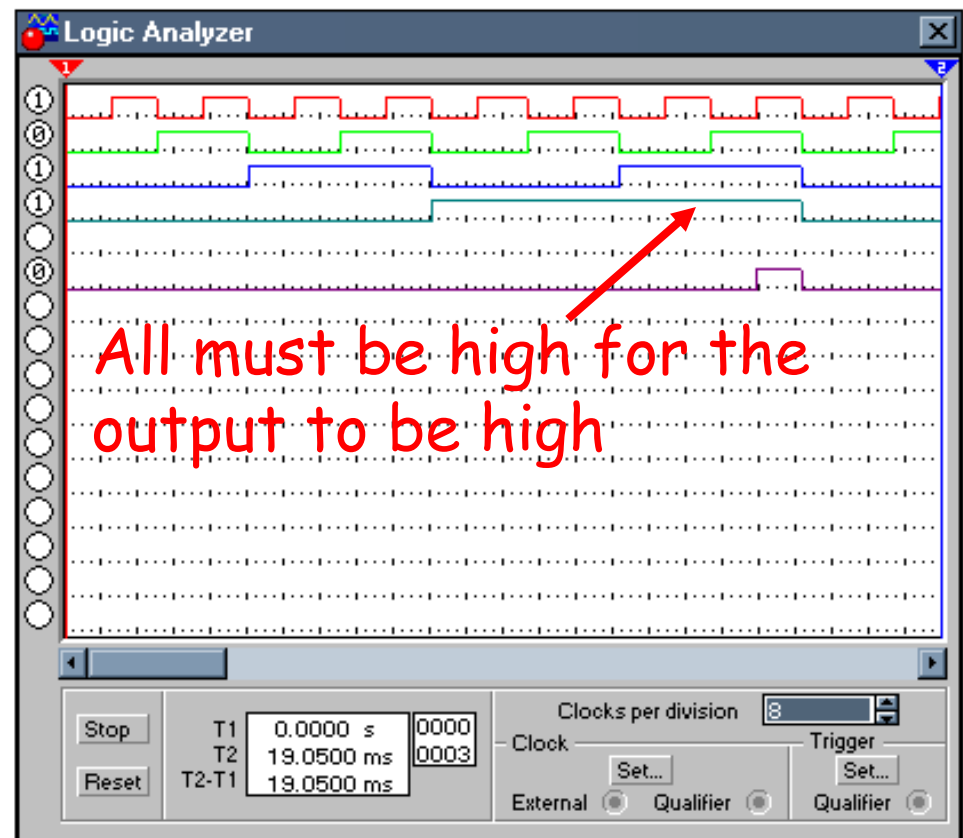
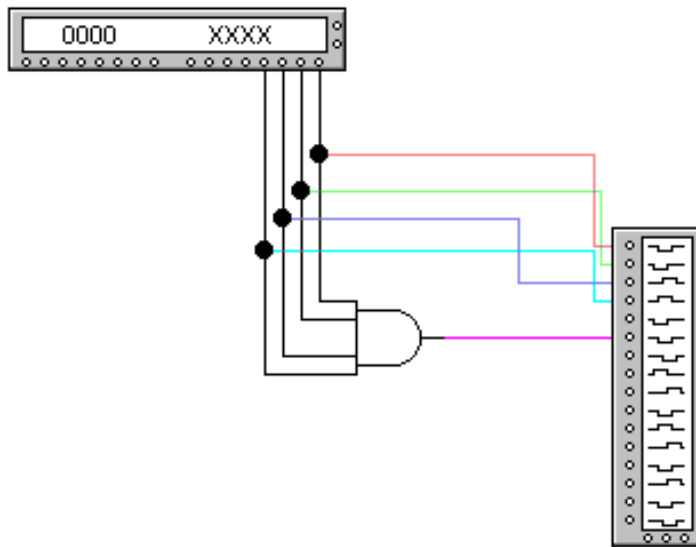
A B X

The figure consists of two parts. On the left is a timing diagram with four horizontal axes labeled A, B, C, and X. The vertical axis represents time, with vertical dashed lines indicating specific time intervals. Signal A is a periodic square wave. Signal B is a square wave that is high for the first two intervals of each period of A and low for the next two. Signal C is low for the first four intervals and then becomes high. Signal X is green and is high only during the first two intervals of each period of A, which corresponds to the periods when both A and B are high. On the right is a logic circuit diagram of a 3-input AND gate. The inputs are labeled A, B, and C. The output is labeled X. The output line X is connected back to the timing diagram, indicating that the output signal X is the logical AND of inputs A, B, and C.

AND 게이트(AND Gate)



AND 게이트의 타이밍 도



All must be high for the output to be high

AND 게이트(AND Gate)



AND 게이트의 논리식 ;

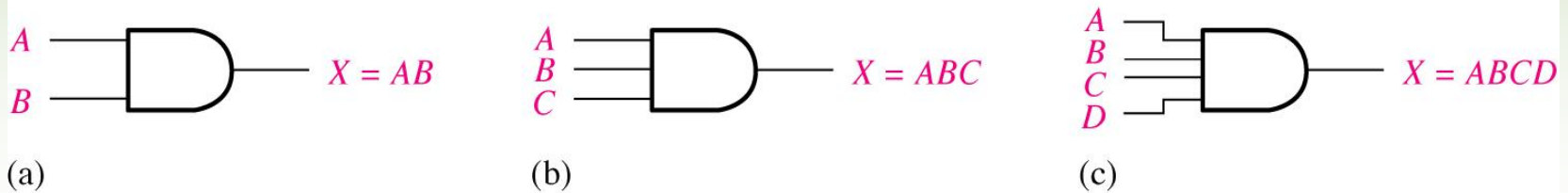


Figure 3-14 Boolean expressions for AND gates with two, three, and four inputs.

Input A	Input B	Output X
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	0	$1 \cdot 0 = 0$
1	1	$1 \cdot 1 = 1$

AND 게이트(AND Gate)



응용 예 ; Enable/Inhibit 소자로서의 AND 게이트

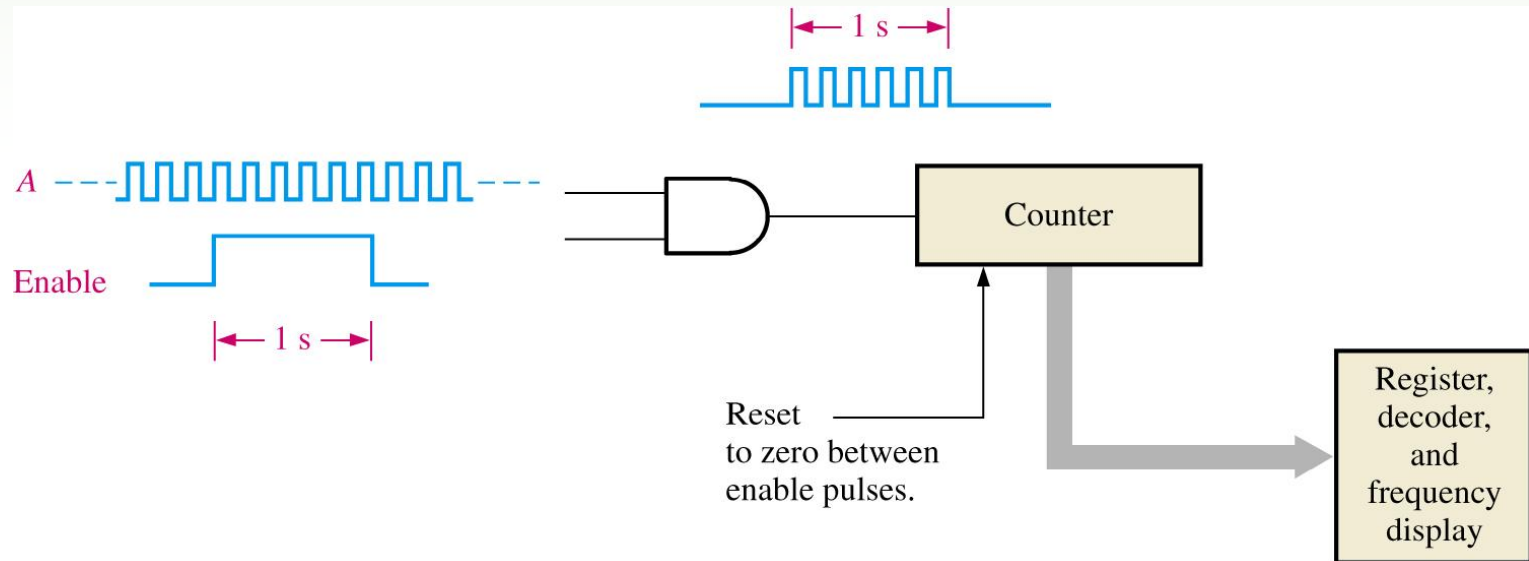


Figure 3-15 An AND gate performing an enable/inhibit function for a frequency counter.

AND 게이트(AND Gate)



응용 예 ; 시트 벨트 경보 시스템

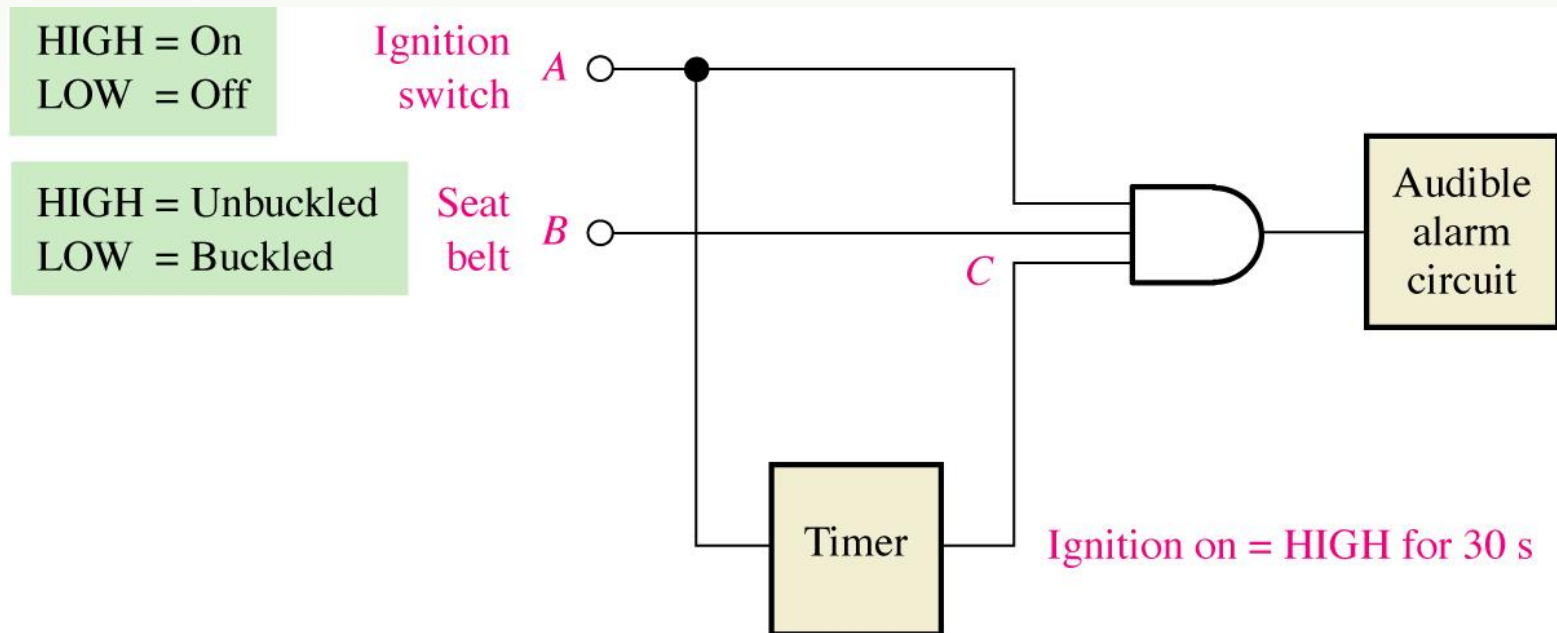
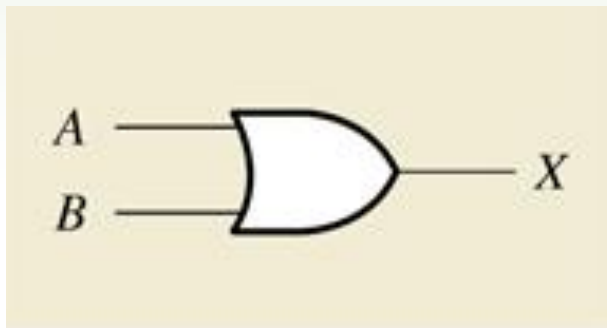


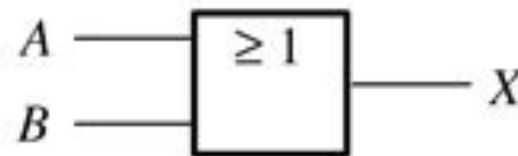
Figure 3-16 A simple seat belt alarm circuit using an AND gate.

OR 게이트(OR Gate)

표준 논리 기호



(a) Distinctive shape



(b) Rectangular outline
with the OR (≥ 1)
qualifying symbol

Figure 3-17 Standard logic symbols for the OR gate showing two inputs (ANSI/IEEE Std. 91-1984).

OR 게이트(OR Gate)



OR 게이트의 연산

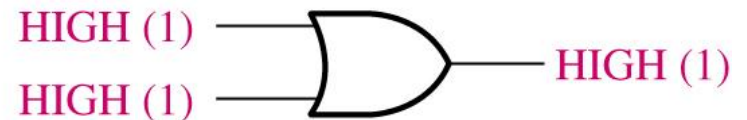
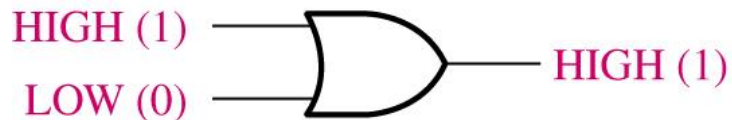


Figure 3-18 All possible logic levels for a 2-input OR gate.

OR 게이트(OR Gate)



OR 게이트의 진리표

Input A	Input B	Output X
Low (0)	Low (0)	Low (0)
Low (0)	High (1)	High (1)
High (1)	Low (0)	High (1)
High (1)	High (1)	High (1)

OR 게이트(OR Gate)



OR 게이트의 펄스 연산

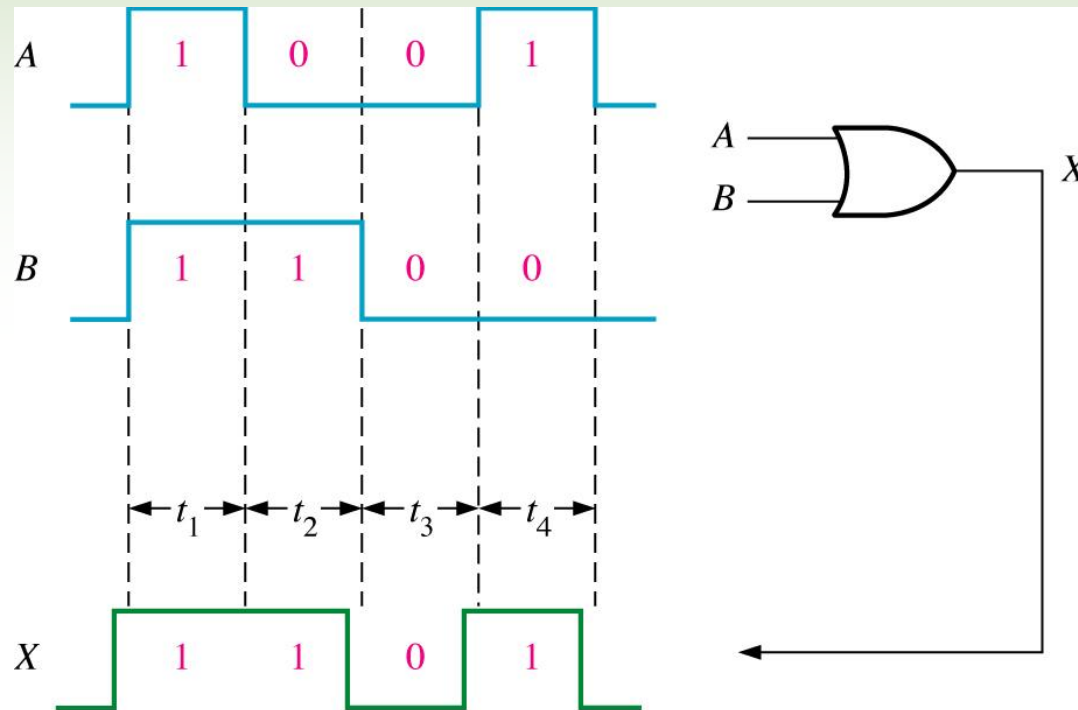
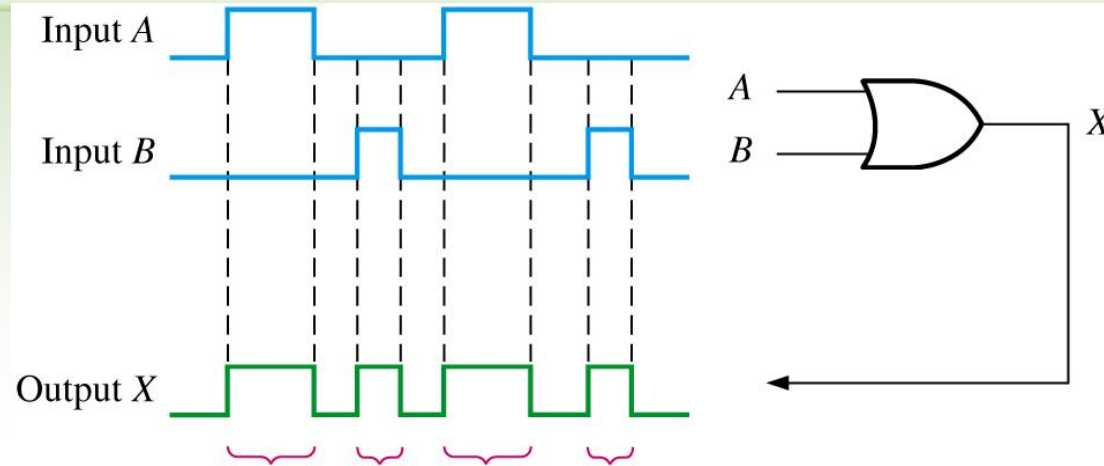


Figure 3-19 Example of pulsed OR gate operation with a timing diagram showing input and output time relationships.

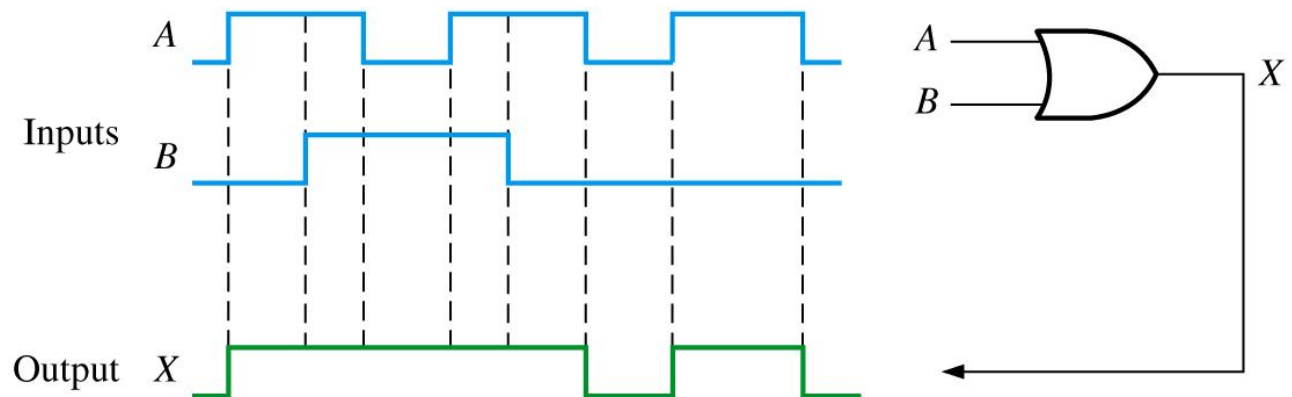
OR 게이트(OR Gate)

예제 3-6)



When either input or both inputs are HIGH,
the output is HIGH.

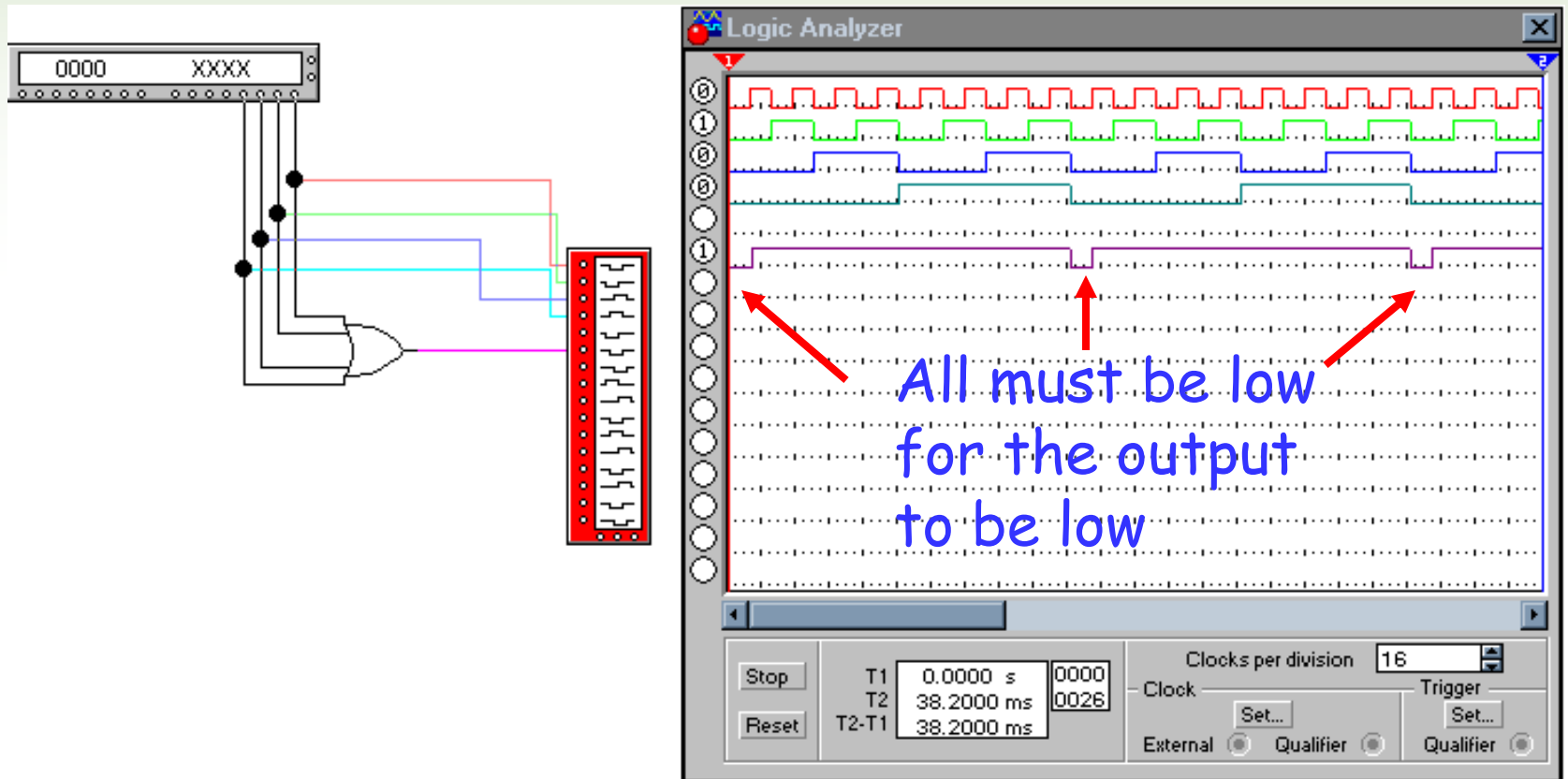
예제 3-7)



OR 게이트(OR Gate)



OR 게이트의 타이밍 도



OR 게이트(OR Gate)



OR 게이트의 논리식 ;

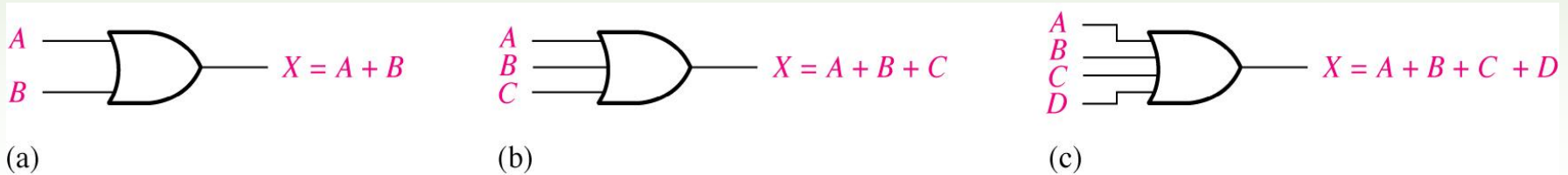


Figure 3-23 Boolean expressions for OR gates with two, three, and four inputs.

Input A	Input B	Output X
0	0	$0 + 0 = 0$
0	1	$0 + 1 = 1$
1	0	$1 + 0 = 1$
1	1	$1 + 1 = 1$

OR 게이트(OR Gate)



응용 예 ; 침입 검출 시스템

Open door/window
sensors

HIGH = Open
LOW = Closed

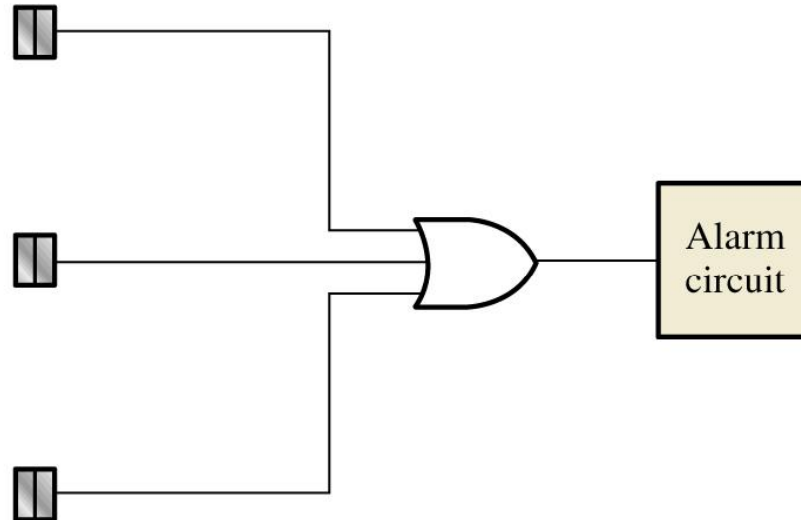
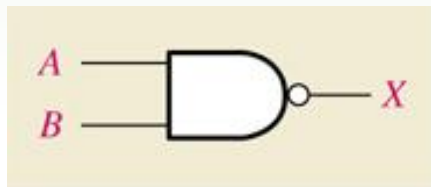


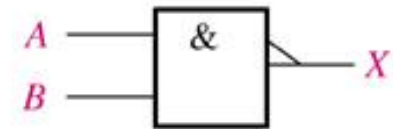
Figure 3-24 A simplified intrusion detection system using an OR gate.

NAND 게이트(NAND Gate)

표준 논리 기호



(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent



(b) Rectangular outline, 2-input NAND gate with polarity indicator

Figure 3-25 Standard NAND gate logic symbols (ANSI/IEEE Std. 91-1984).

NAND 게이트(NAND Gate)



● NAND 게이트의 연산

LOW (0)
LOW (0) —  — HIGH (1)

LOW (0)
HIGH (1) —  — HIGH (1)

HIGH (1)
LOW (0) —  — HIGH (1)

HIGH (1)
HIGH (1) —  — LOW (0)

Figure 3-26 Operation of a 2-input NAND gate.

NAND 게이트(NAND Gate)



● NAND 게이트의 진리표

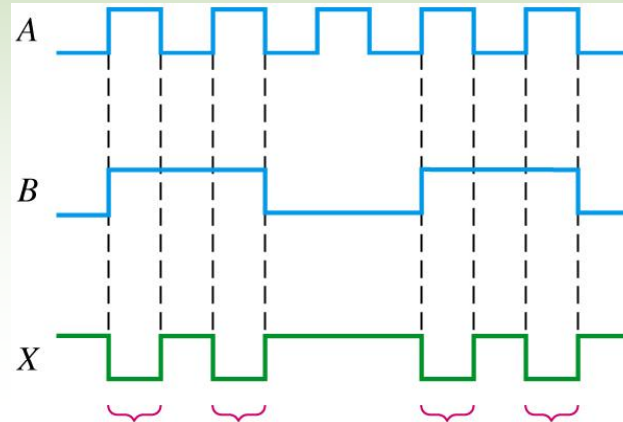
Input A	Input B	Output X
Low (0)	Low (0)	High (1)
Low (0)	High (1)	High (1)
High (1)	Low (0)	High (1)
High (1)	High (1)	Low (0)

NAND 게이트(NAND Gate)

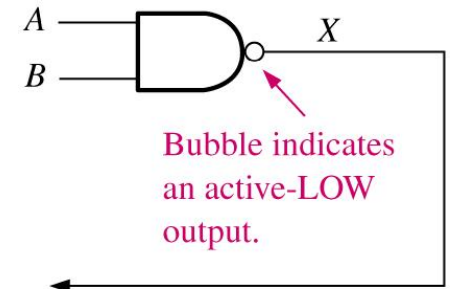


NAND 게이트 의 펄스 연산

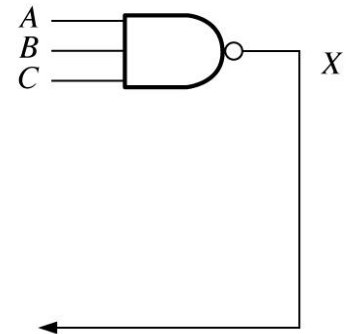
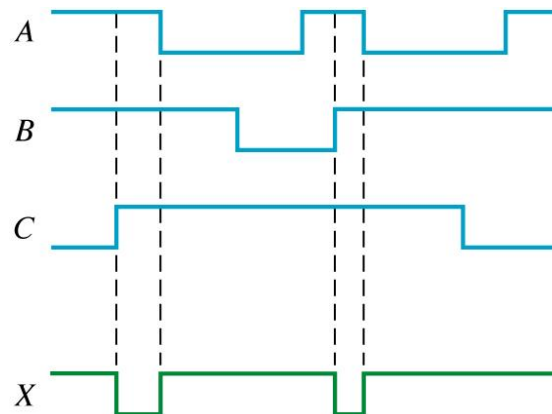
EX 3-9)



A and B are both HIGH during these four time intervals. Therefore X is LOW.



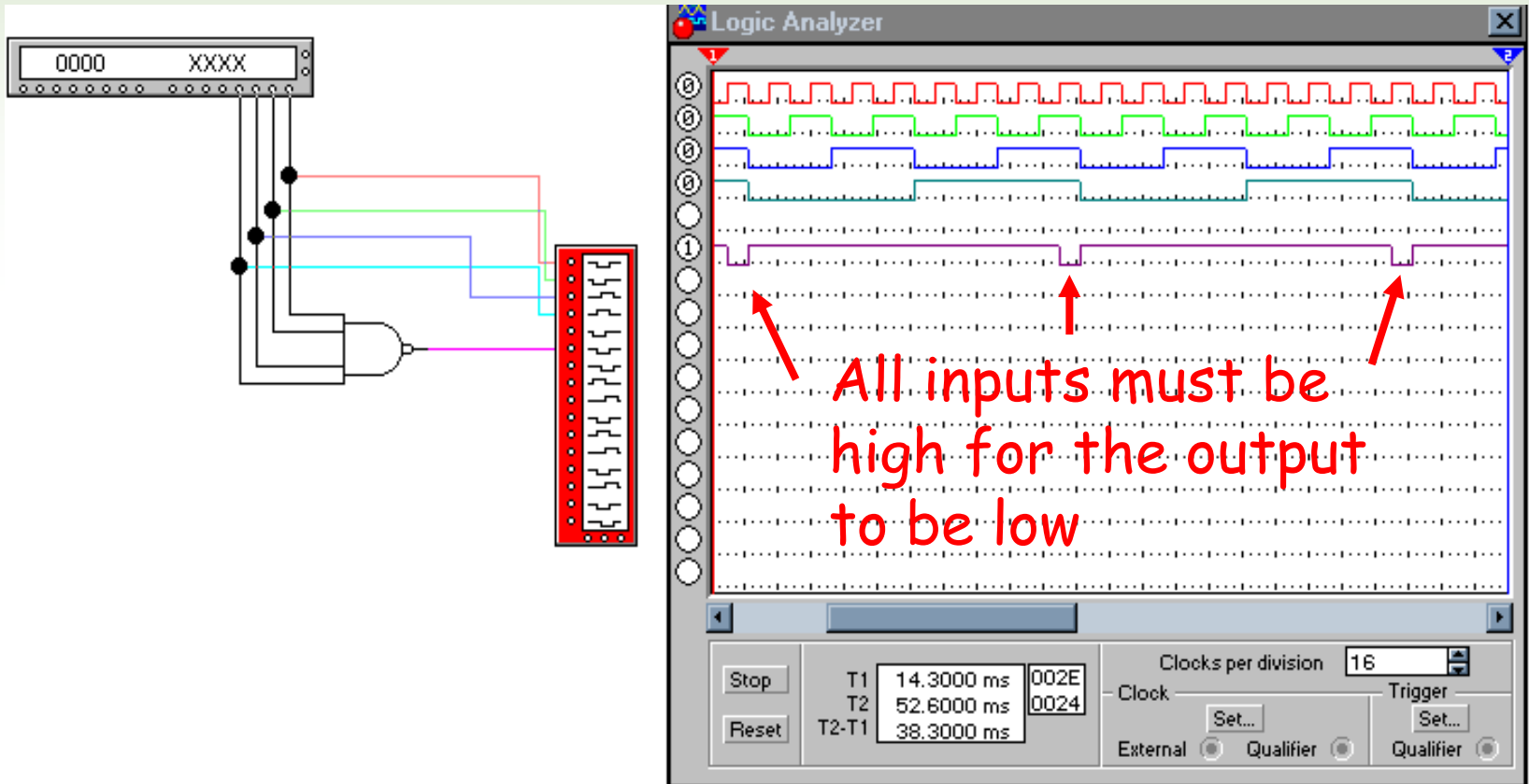
EX 3-10)



NAND 게이트(NAND Gate)



NAND 게이트의 타이밍 도



NAND 게이트(NAND Gate)



● NAND 게이트의 등가성

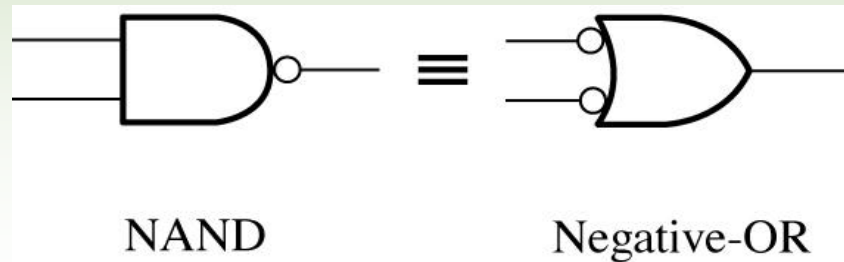


Figure 3-29 Standard symbols representing the two equivalent operations of a NAND gate.

● NAND 게이트 의 논리식 ;

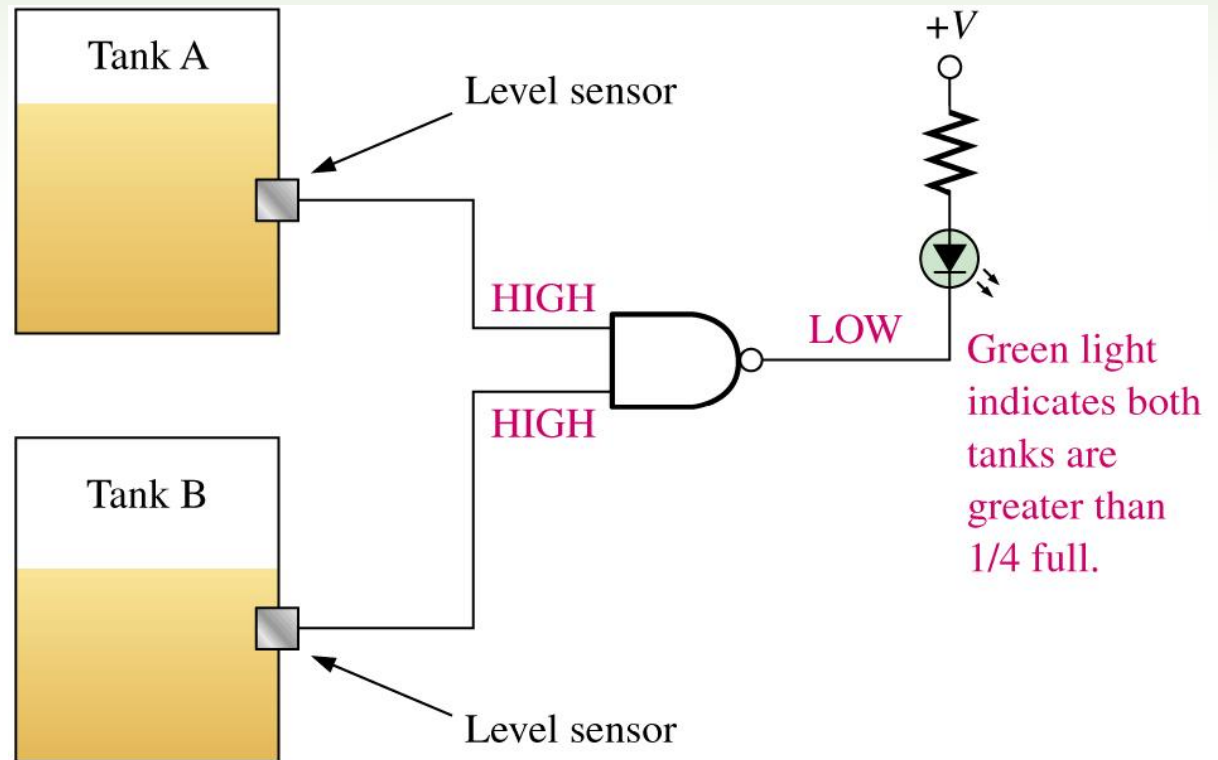
Input A	Input B	Output X
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

NAND 게이트(NAND Gate)



응용 예 ; (예제 3-11) 레벨 검출 시스템

두 개의 탱크 모두
전체의 $\frac{1}{4}$ 레벨 이상인
것을 감지하고자 할 때

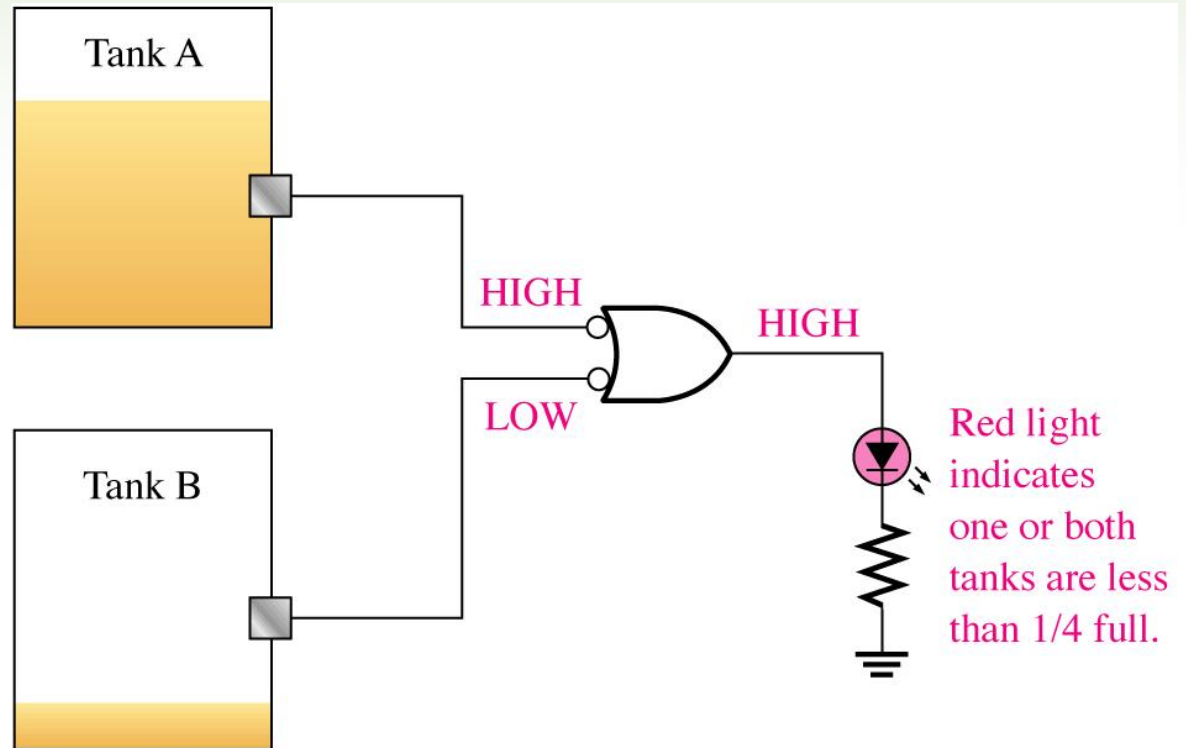


NAND 게이트(NAND Gate)



- 응용 예 ; (예제 3-12) 레벨 검출 시스템

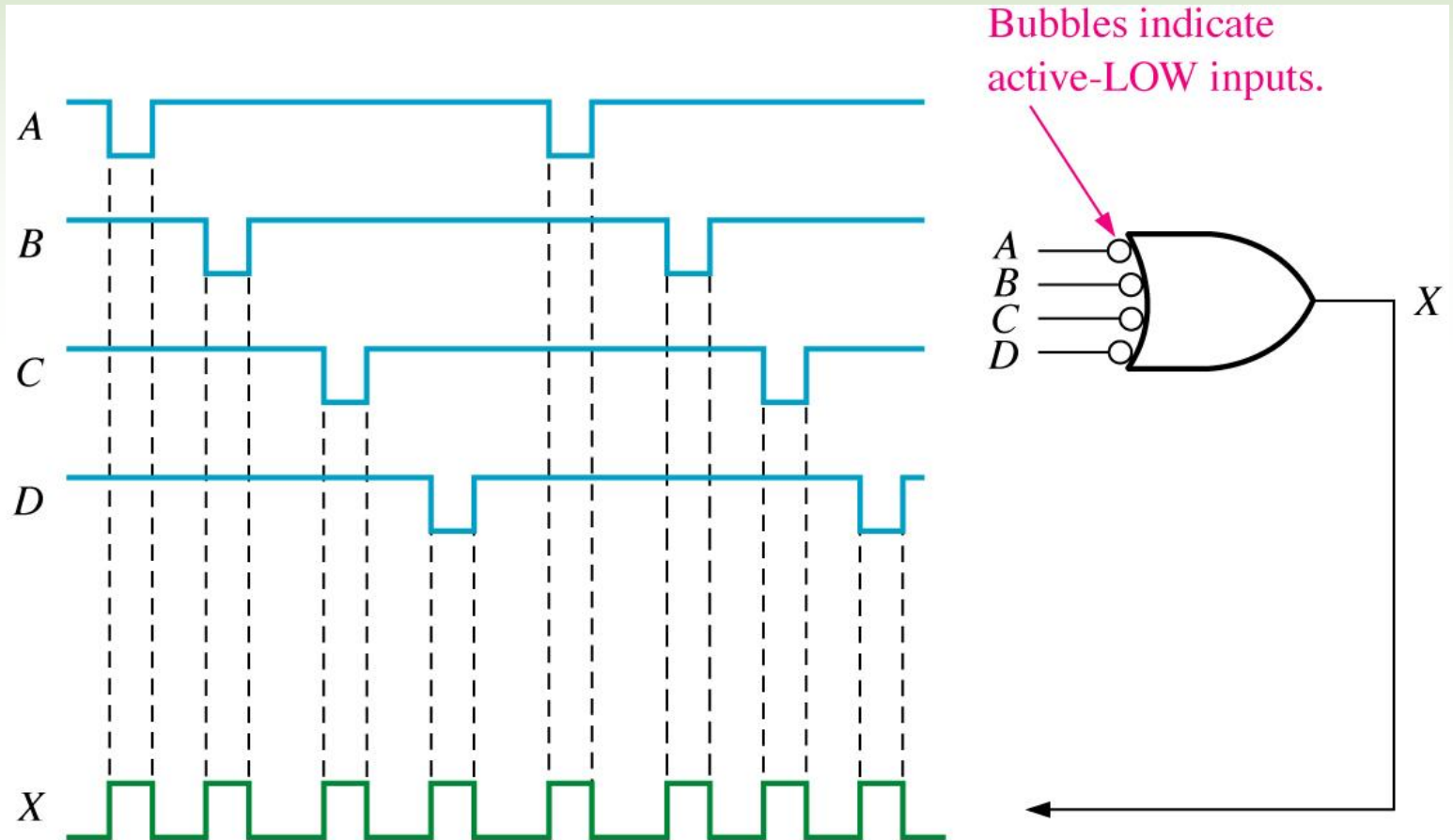
적어도 한 개의 탱크가
전체의 1/4 레벨 이하인
것을 감지하고자 할 때



NAND 게이트(NAND Gate)

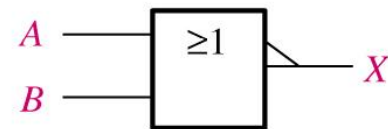
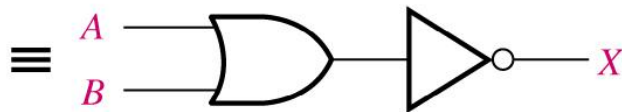
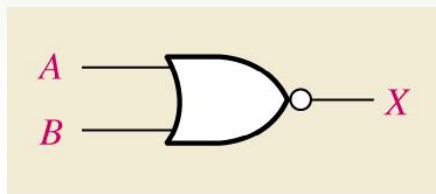


(예제 3-13) 부-OR(Negative-OR) 4 입력 NAND 게이트



NOR 게이트(NOR Gate)

표준 논리 기호



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent

(b) Rectangular outline, 2-input NOR gate with polarity indicator

Figure 3–33 Standard NOR gate logic symbols (ANSI/IEEE Std. 91–1984).

NOR 게이트(NOR Gate)



● NOR 게이트의 연산

LOW (0)
LOW (0) → HIGH (1)

LOW (0)
HIGH (1) → LOW (0)

HIGH (1)
LOW (0) → LOW (0)

HIGH (1)
HIGH (1) → LOW (0)

Figure 3-34 Operation of a 2-input NOR gate.

NOR 게이트(NOR Gate)



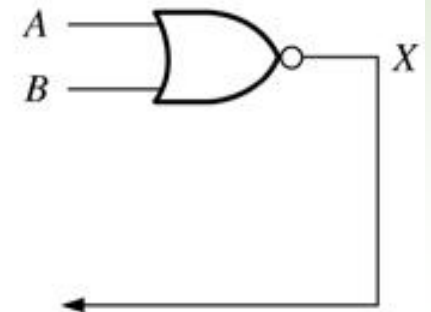
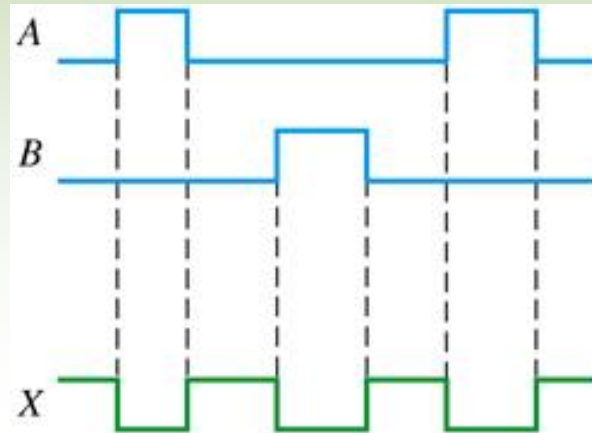
● NOR 게이트의 진리표

Input A	Input B	Output X
Low (0)	Low (0)	High (1)
Low (0)	High (1)	Low (0)
High (1)	Low (0)	Low (0)
High (1)	High (1)	Low (0)

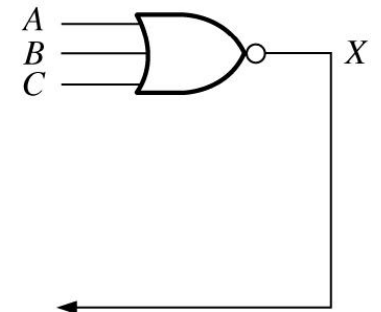
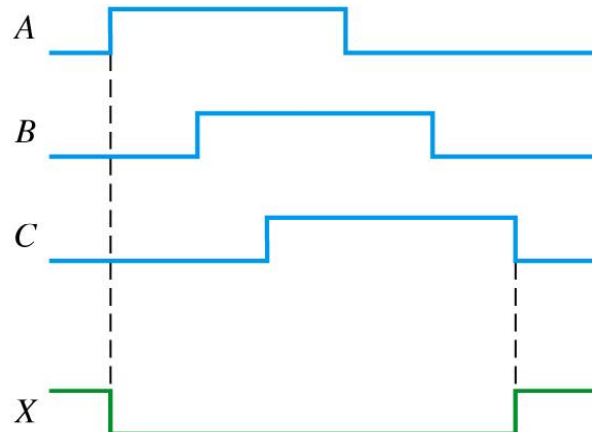
NOR 게이트(NOR Gate)



◎ NOR 게이트
의 펄스 연산
EX 3-14)



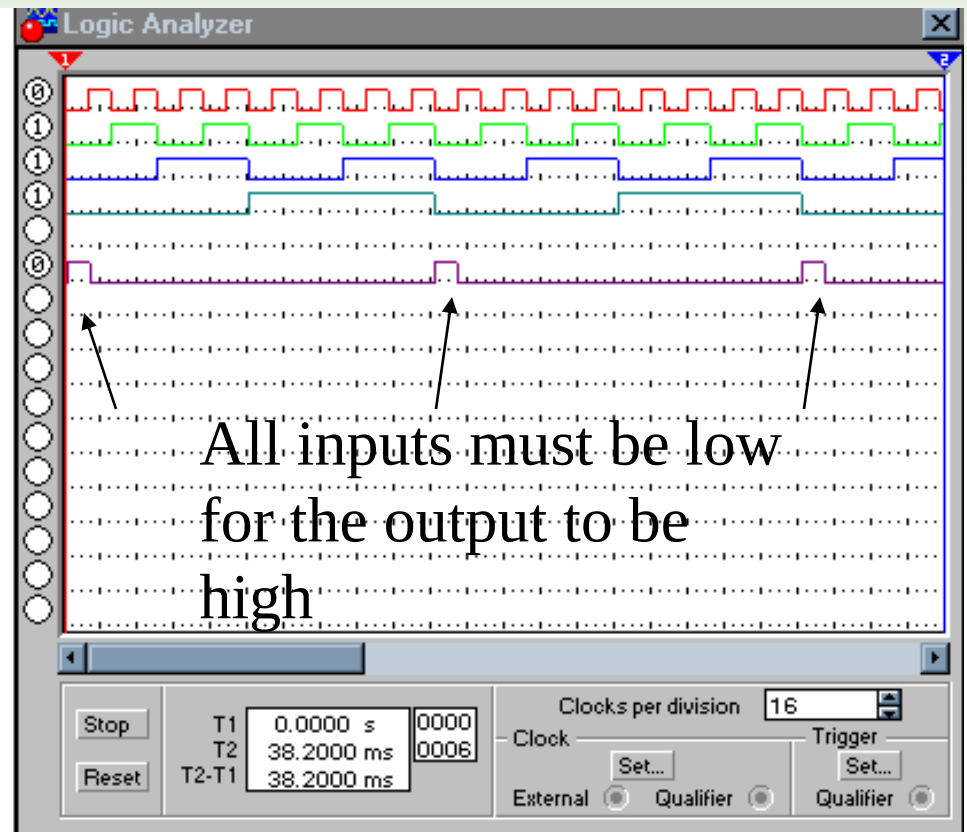
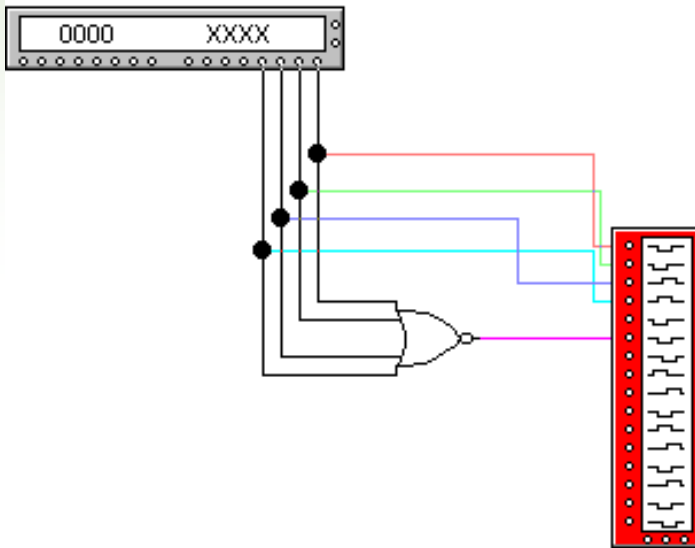
EX 3-15)



NOR 게이트(NOR Gate)



NOR 게이트의 타이밍 도



NOR 게이트(NOR Gate)



● NOR 게이트의 등가성

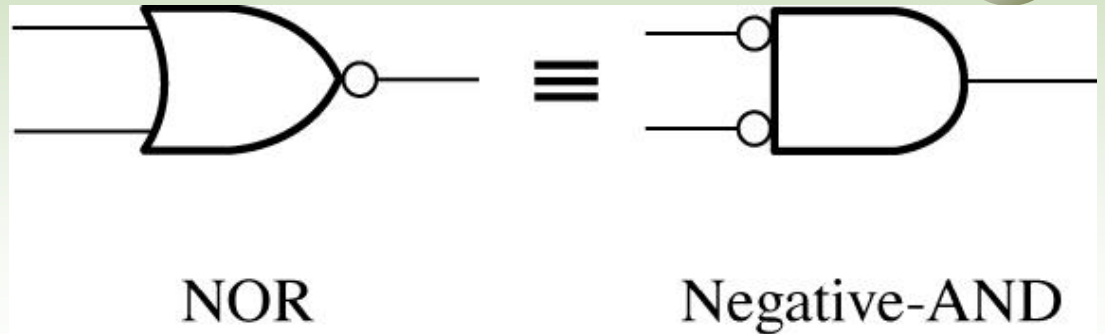


Figure 3-37 Standard symbols representing the two equivalent operations of a NOR gate.

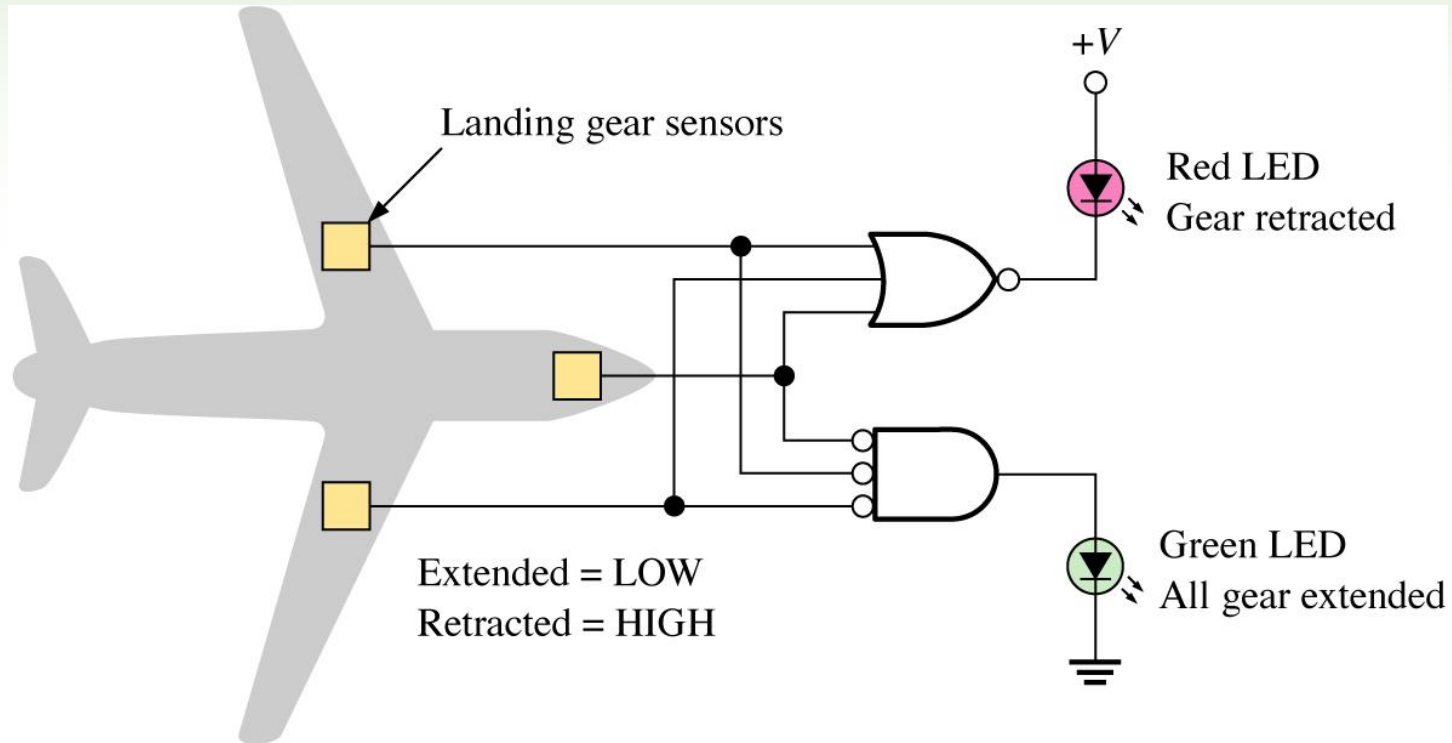
● NOR 게이트의 논리식 ;

Input A	Input B	Output X
0	0	$\overline{0+0} = \overline{0} = 1$
0	1	$\overline{0+1} = \overline{1} = 0$
1	0	$\overline{1+0} = \overline{1} = 0$
1	1	$\overline{1+1} = \overline{1} = 0$

NOR 게이트(NOR Gate)



응용 예 ; (예제 3-17) 랜딩 기어 상태 검출 시스템

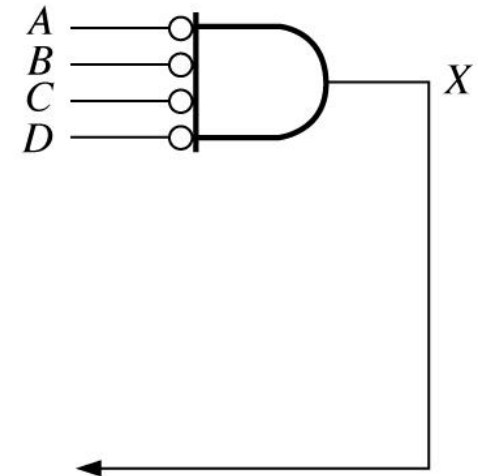
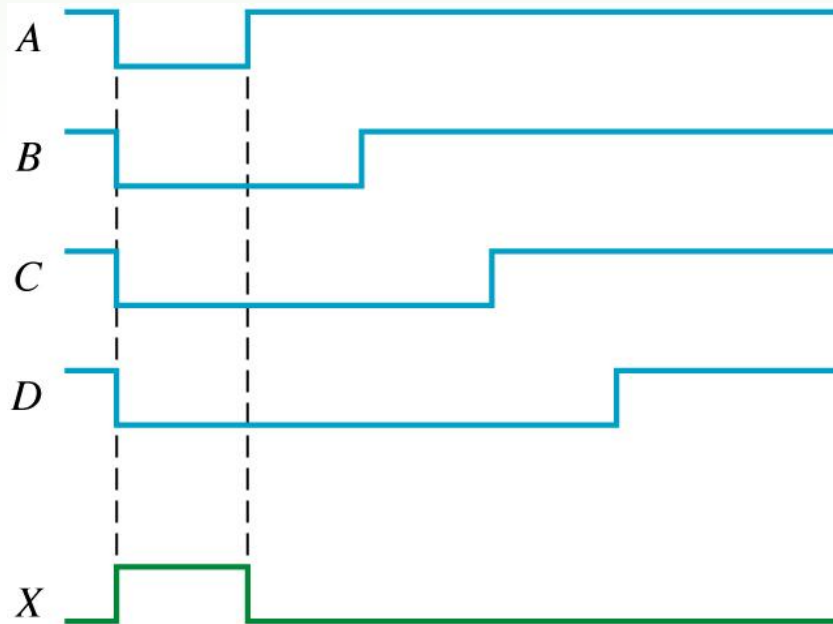


NOR 게이트(NOR Gate)



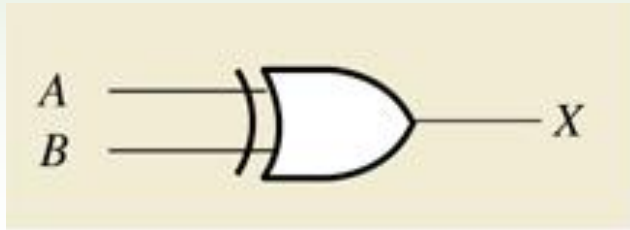
응용 예 ; (예제 3-18)

부-AND(Negative-AND) 4 입력 NOR 게이트

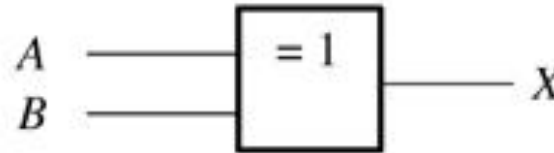


XOR, XNOR 게이트

배타적-OR 게이트의 표준 논리 기호



(a) Distinctive shape



(b) Rectangular outline with the XOR qualifying symbol (= 1)

Figure 3-41 Standard logic symbols for the exclusive-OR gate.

XOR, XNOR 게이트



● XOR 게이트의 연산

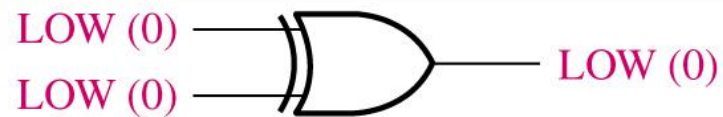


Figure 3-42 All possible logic levels for an exclusive-OR gate.

XOR, XNOR 게이트



● XOR 게이트의 진리표

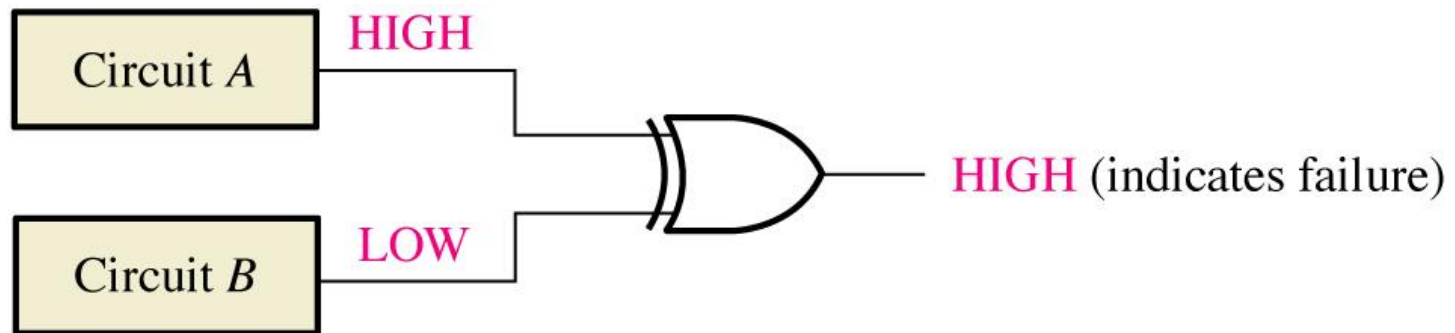
A	B	Output
Low (0)	Low (0)	Low (0)
Low (0)	High (1)	High (1)
High (1)	Low (0)	High (1)
High (1)	High (1)	Low (0)

XOR, XNOR 게이트



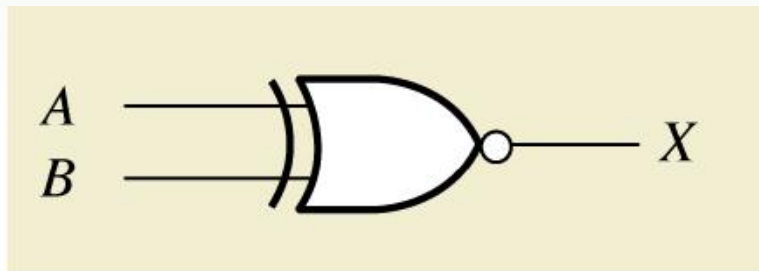
응용 예 ; (예제 3-19) 고장 검출 시스템

병렬동작하는 동일한 두 개의 회로에서의 고장 검출

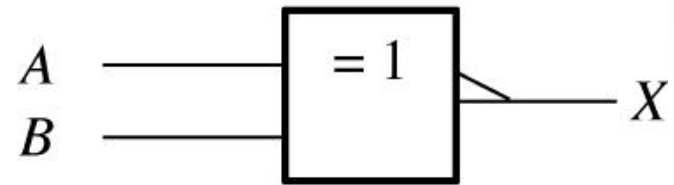


XOR, XNOR 게이트

배타적-NOR 게이트의 표준 논리 기호



(a) Distinctive shape



(b) Rectangular outline

Figure 3-44 Standard logic symbols for the exclusive-NOR gate.

XOR, XNOR 게이트



○ XNOR 게이트의 연산

LOW (0)
LOW (0) → HIGH (1)

LOW (0)
HIGH (1) → LOW (0)

HIGH (1)
LOW (0) → LOW (0)

HIGH (1)
HIGH (1) → HIGH (1)

Figure 3-45 All possible logic levels for an exclusive-NOR gate.

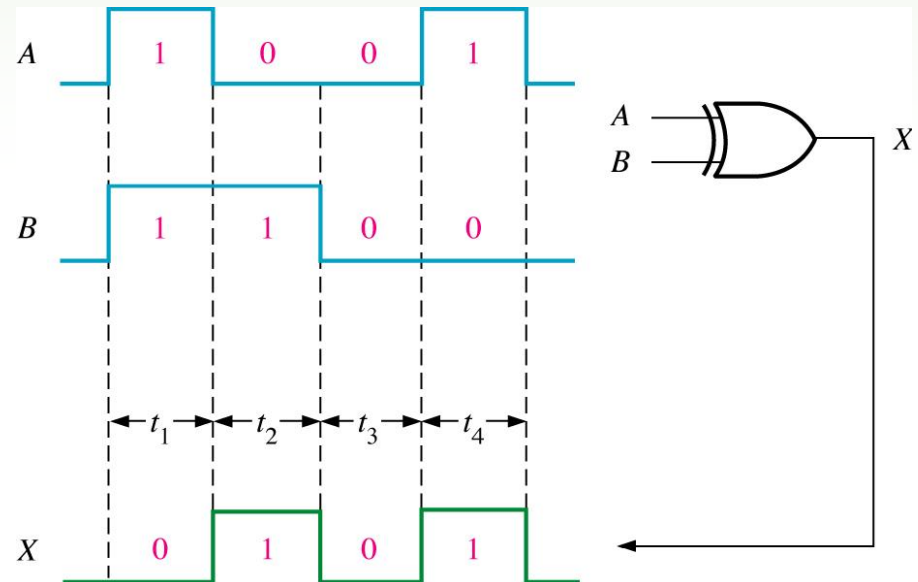
XOR, XNOR 게이트



● XNOR 게이트의 진리표

A	B	Output
Low (0)	Low (0)	High (1)
Low (0)	High (1)	Low (0)
High (1)	Low (0)	Low (0)
High (1)	High (1)	High (1)

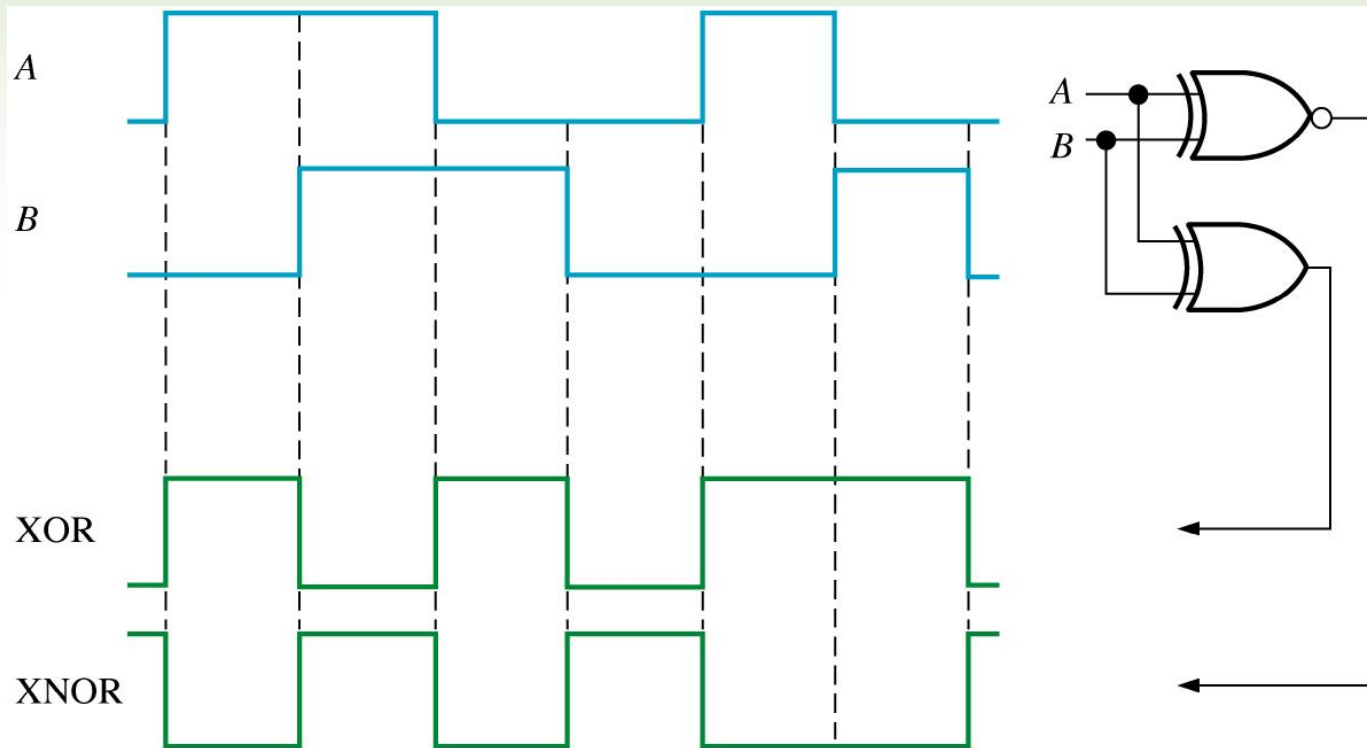
● XNOR 게이트의 펄스 연산



XOR, XNOR 게이트



(예제 3-20)

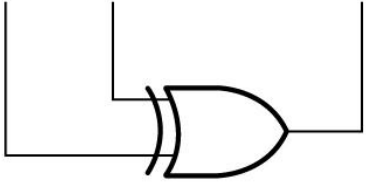


XOR, XNOR 게이트



응용 예 ; XOR를 사용한 2-비트 덧셈기

Input bits		Output (sum)
A	B	Σ
0	0	0
0	1	1
1	0	1
1	1	0 (without 1 carry)



The diagram shows an XOR gate with two inputs and one output. The inputs are connected to the two lines entering the gate from the left, and the output is connected to the line exiting the gate to the right.

Figure 3-48 An XOR gate used to add two bits.