디지털 시스템 : 기초 및 VHDL

1. 디지털 개념 입문
2. 수 체계, 연산 및 코드
3. 논리 게이트
4. 부울 대수와 논리 간소화
5. 조합 논리
6. 조합 논리의 기능
7. 플립-플롭과 관련 소자
8. 카운터
9. (시프트 레지스터)

1장. 디지털 개념 입문

- 디지털 및 아날로그 양 (1)
- 2진 디지트, 논리레벨, 디지털 파형(2)
- 논리 연산 및 논리 함수(3, 4)
- 고정-기능 집적회로(5)
- 프로그래머블 논리의 기초(6)
- 프로그래밍(7)
- (VHDL, 테스트 장비 입문, 8,9)

아날로그 양(Analog Quantity)

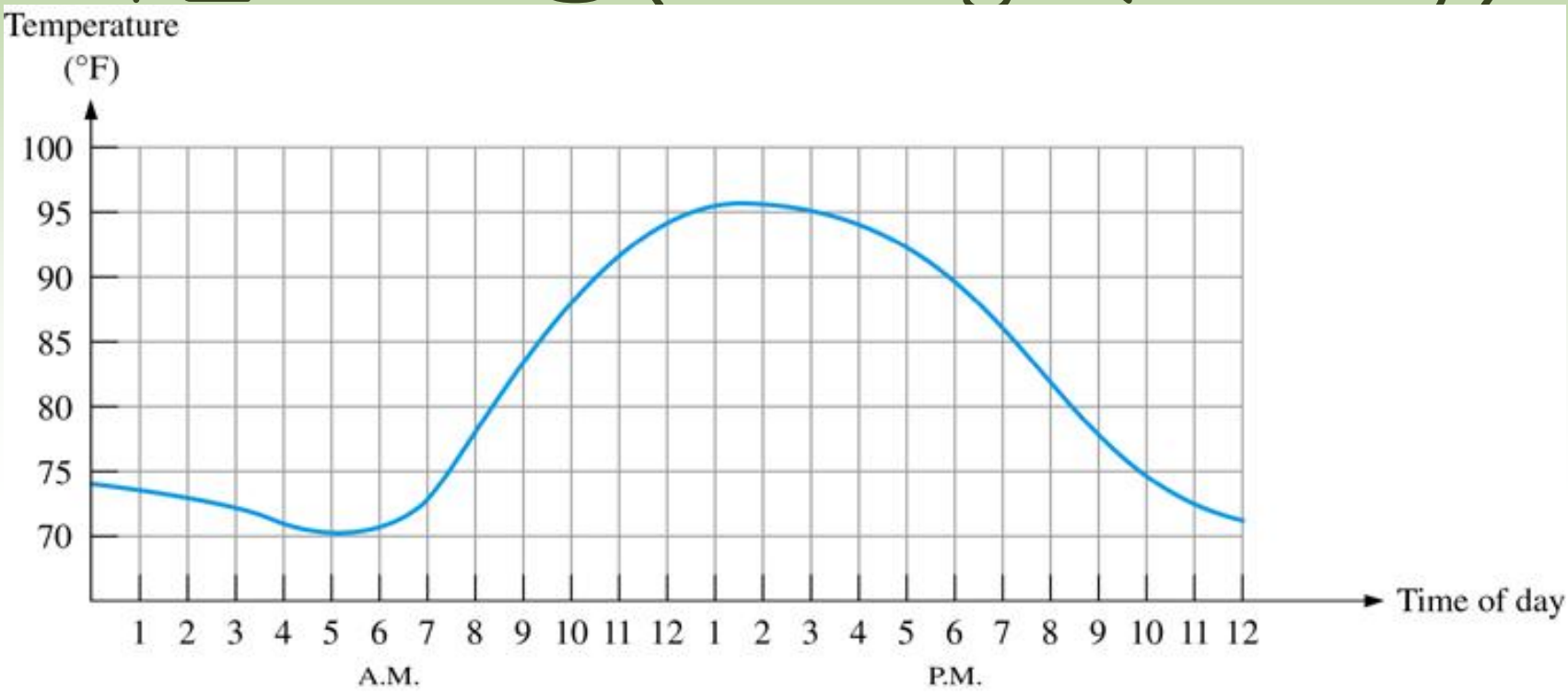


Figure 1–1 Graph of an analog quantity (temperature versus time)

디지털 양(Digital Quantity)

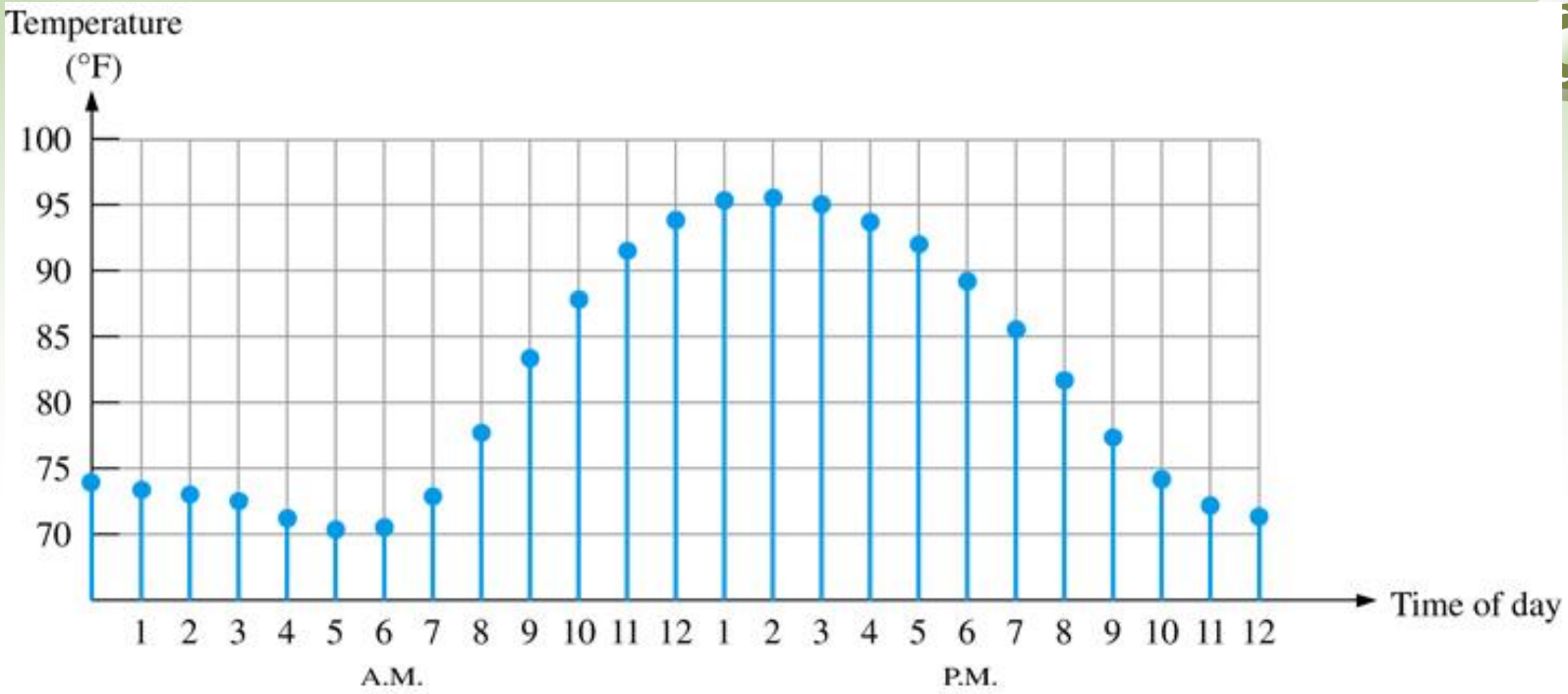


Figure 1-2 Sampled-value representation (quantization) of the an alog quantity in Figure 1-1. Each value represented by a dot can be digitized by representing it as a digital code that

디지털의 장점

아날로그 전자회로 시스템

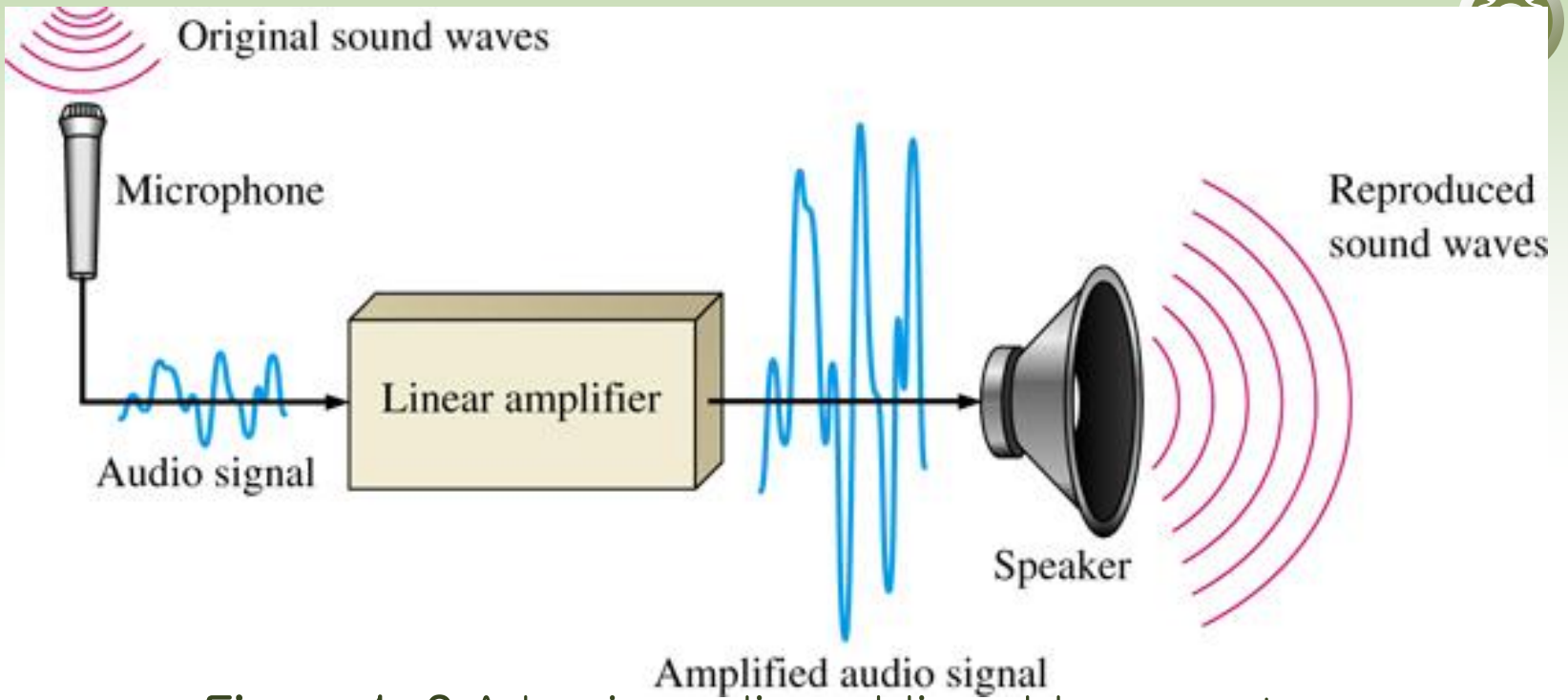


Figure 1-3 A basic audio public address system.

- 마이크 :
- 스피커 :
- 선형 증폭기 :

디지털과 아날로그를 사용하는 시스템

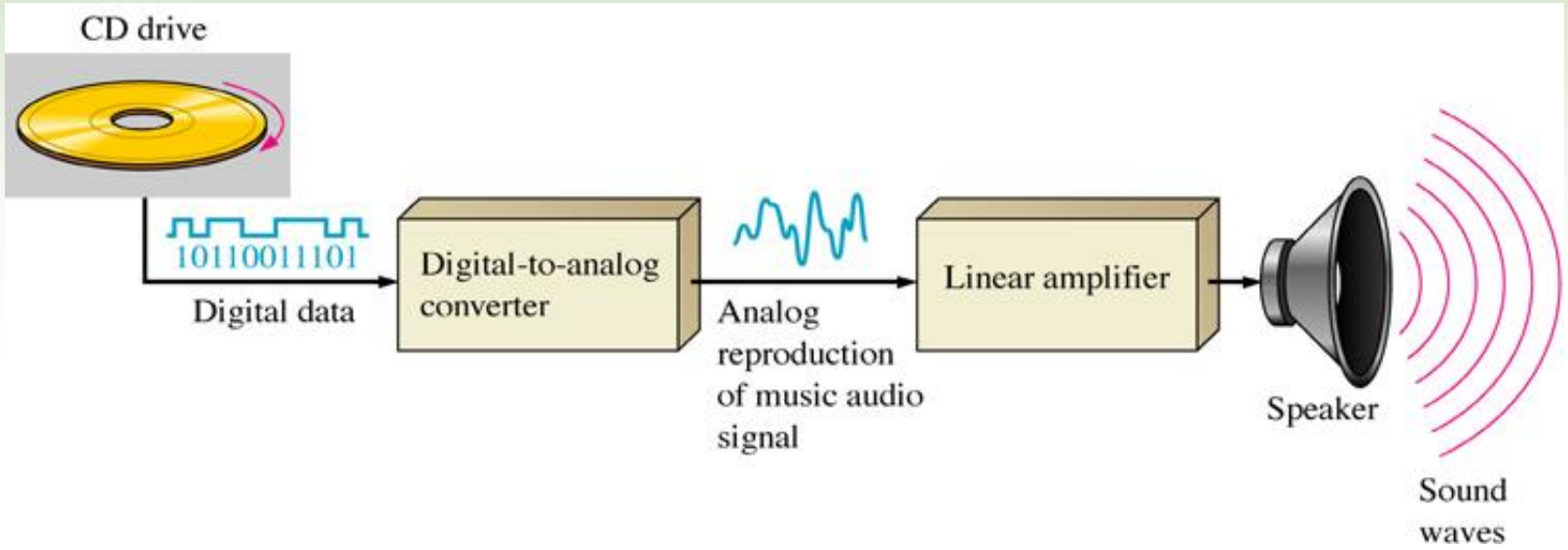


Figure 1-4 Basic principle of a CD player. Only one channel is shown.

2진 디지트, 논리레벨, 디지털 파형

- 디지털 전자 회로(공학)
  - 다루는 신호는 2개의 상태만을 갖는다.
    - 전압, 전류 ; High, Low
    - 스위치 상태 ; 닫힘, 열림
    - 전등의 상태 ; 켜짐, 꺼짐

    ⇒ 2개의 상태를 나타내는 수체계를 2진수 체계라 한다.

2진 디지트(Binary Digit)

- 2진 디지트(Binary Digit) ; Bit
  - 1 과 0
    - 정논리(positive logic)
    - 부논리(negative logic)
  - 코드 :

    예) A(=1000001)

논리 레벨

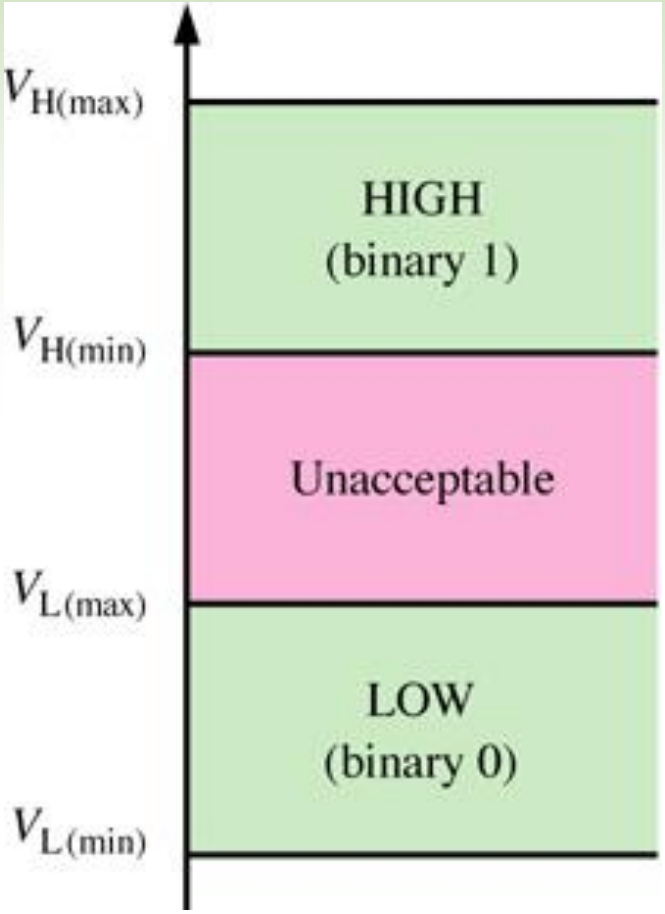


Figure 1–5 Logic level ranges of voltage for a digital circuit.

디지털 파형 및 이상적인 펄스

- 이상적인 펄스
  - 레벨이

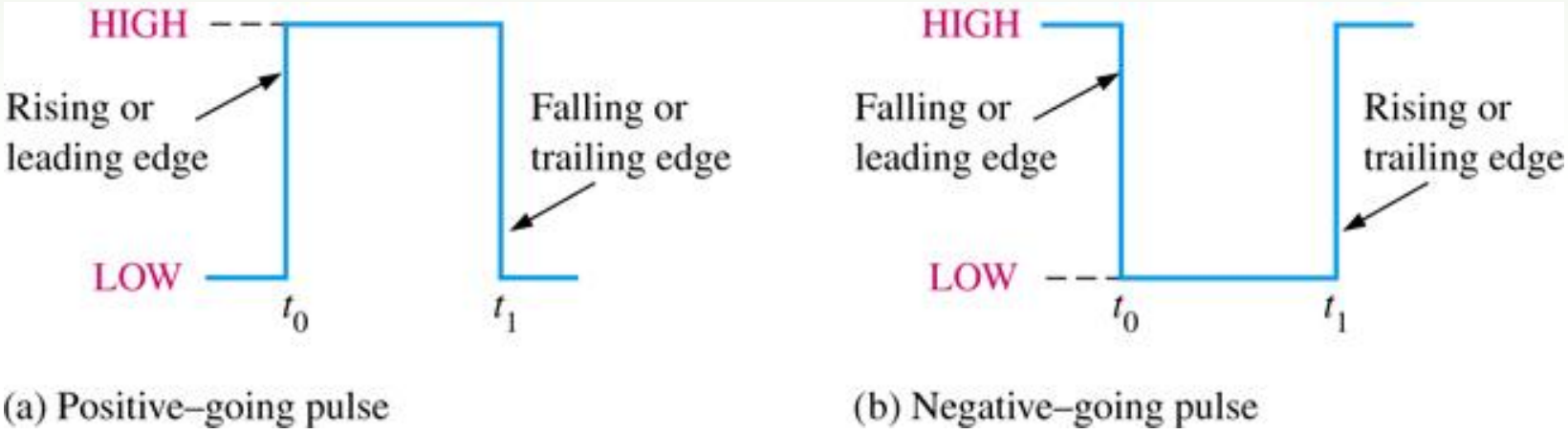


Figure 1-6 Ideal pulses.

비이상적인 펄스(실제적인 펄스)

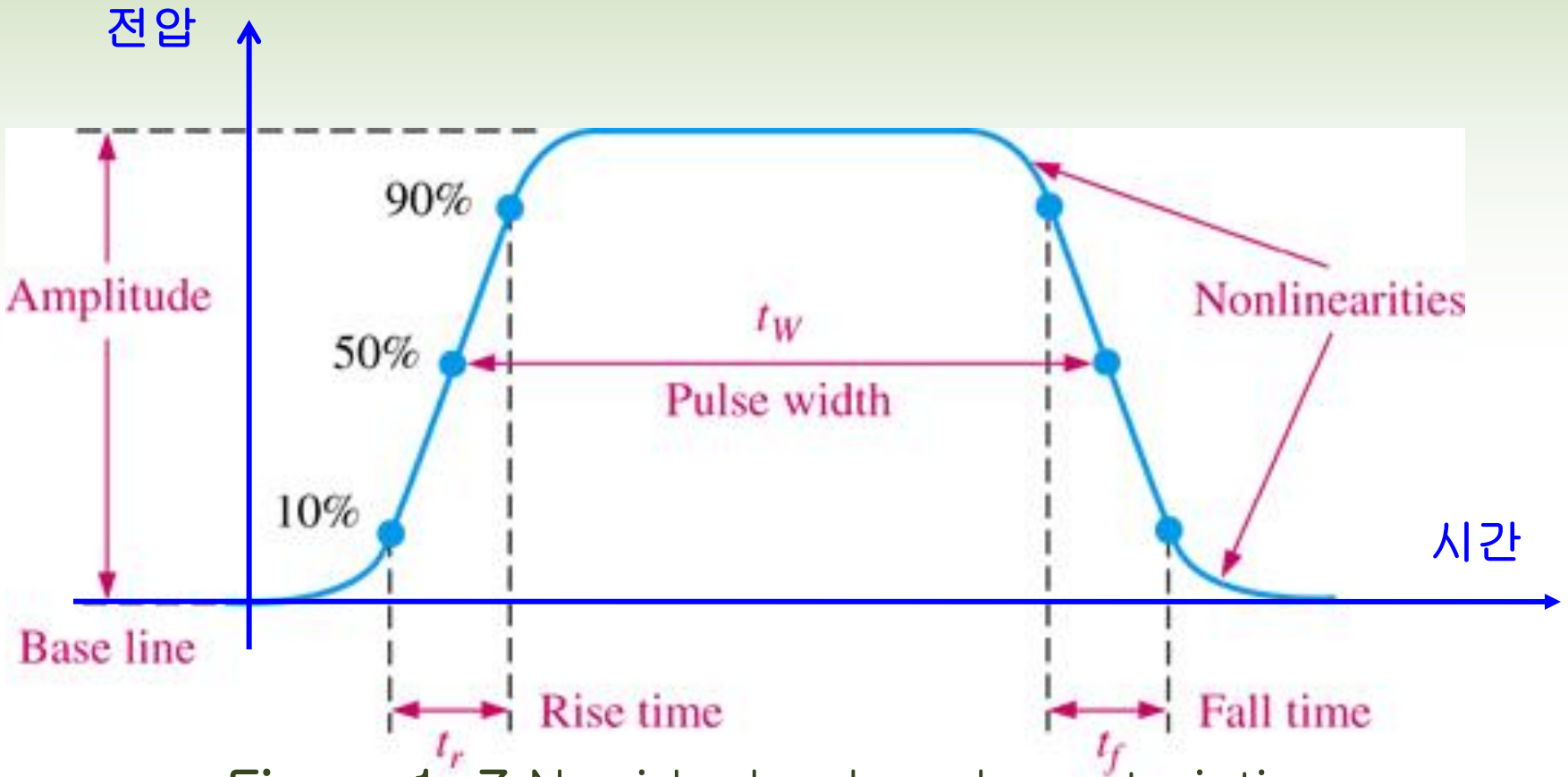
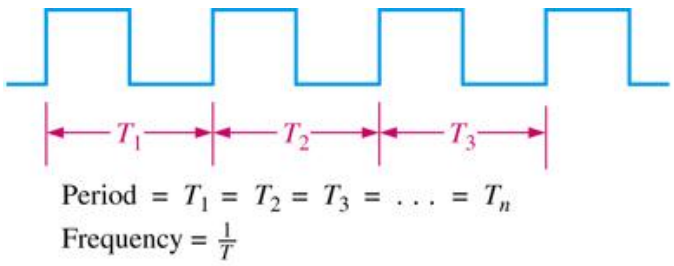


Figure 1-7 Nonideal pulse characteristics.

파형의 특성

- 주기펄스 파형

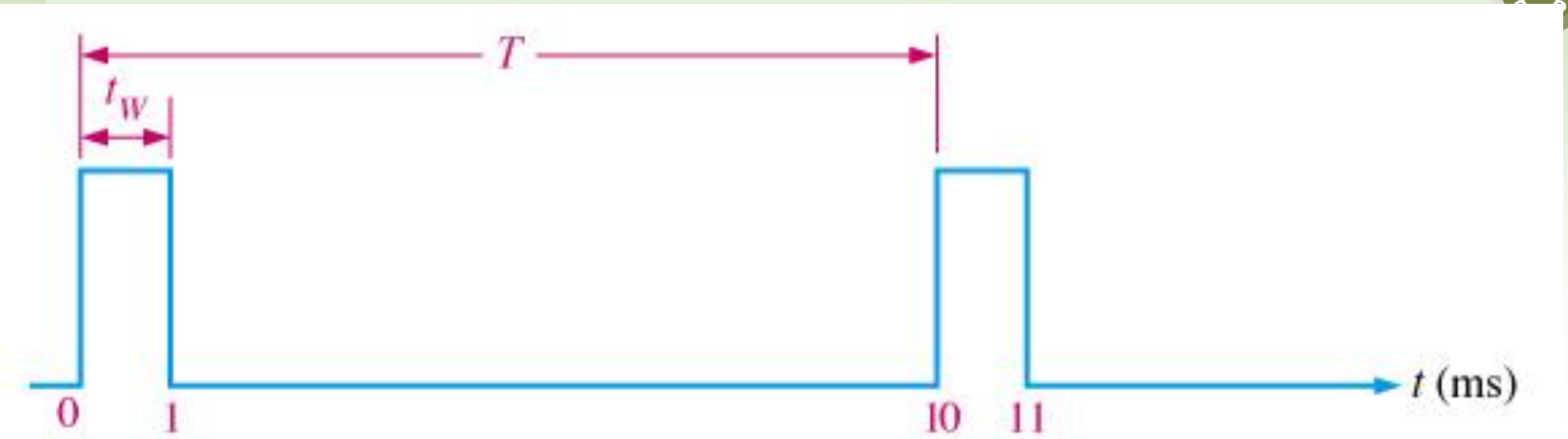


(a) Periodic (square wave)

(b) Nonperiodic

Figure 1-8 Examples of digital waveforms.

예제1-1



2진 정보를 전송하는 디지털 파형

- 클럭(clock, 시계) :
  - 디지털 시스템에서의 모든 파형은

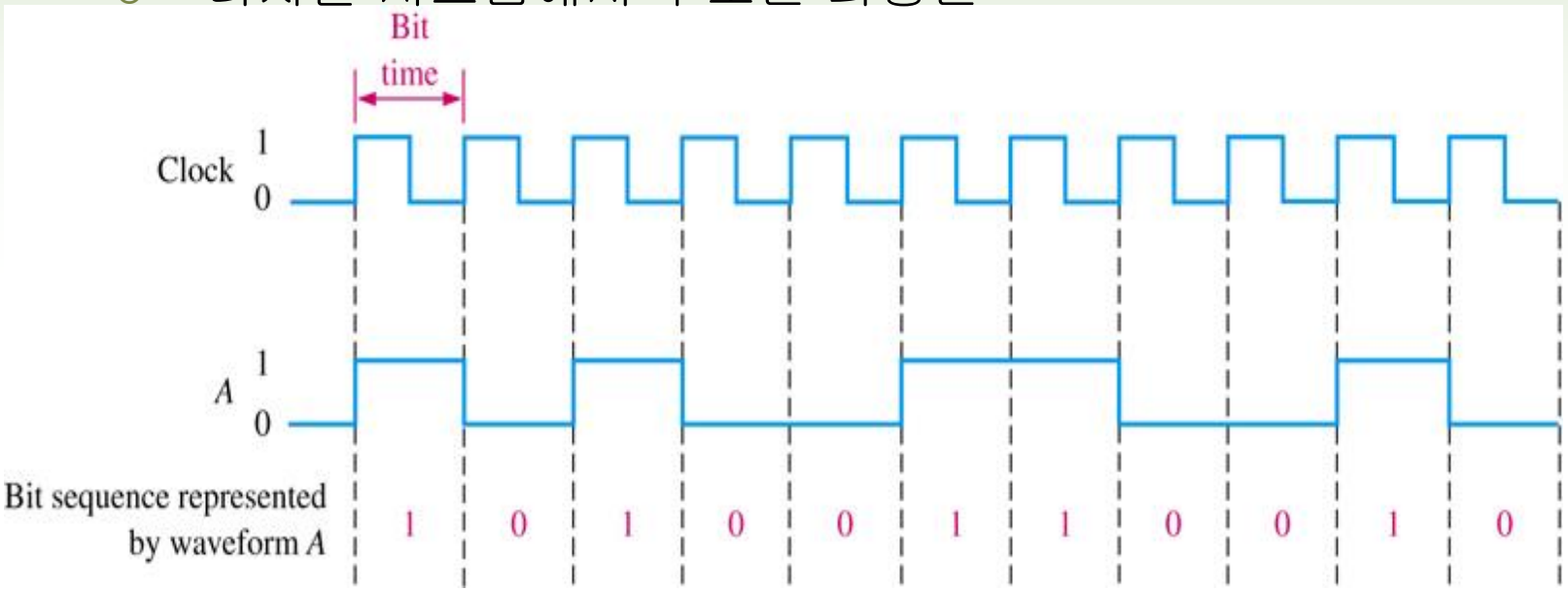


Figure 1-10 Example of a clock waveform synchronized with a waveform representation of a sequence of bits. (rising edge case)

타이밍도(Timing Diagram)

- 타이밍도 : 시간에 따라 둘 이상의 디지털 파형들이 어떻게 변화하는가를 그림으로 나타낸 것.

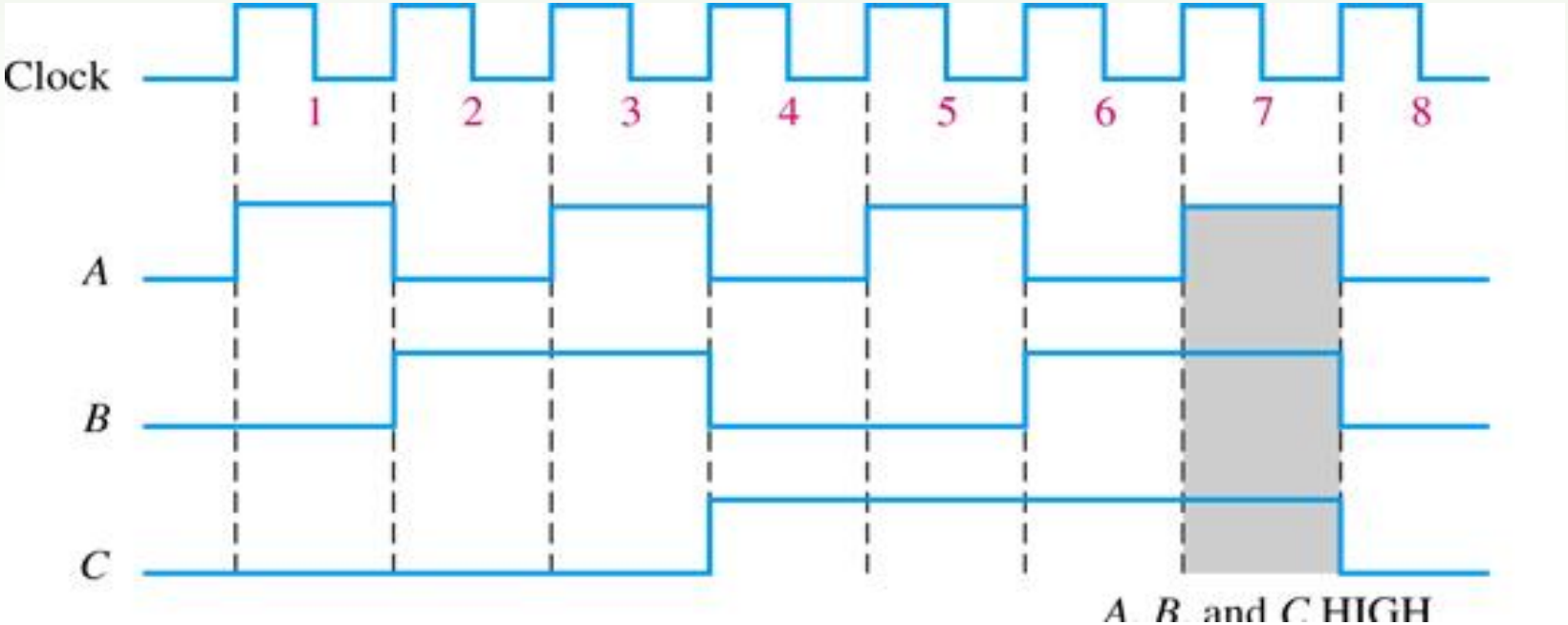
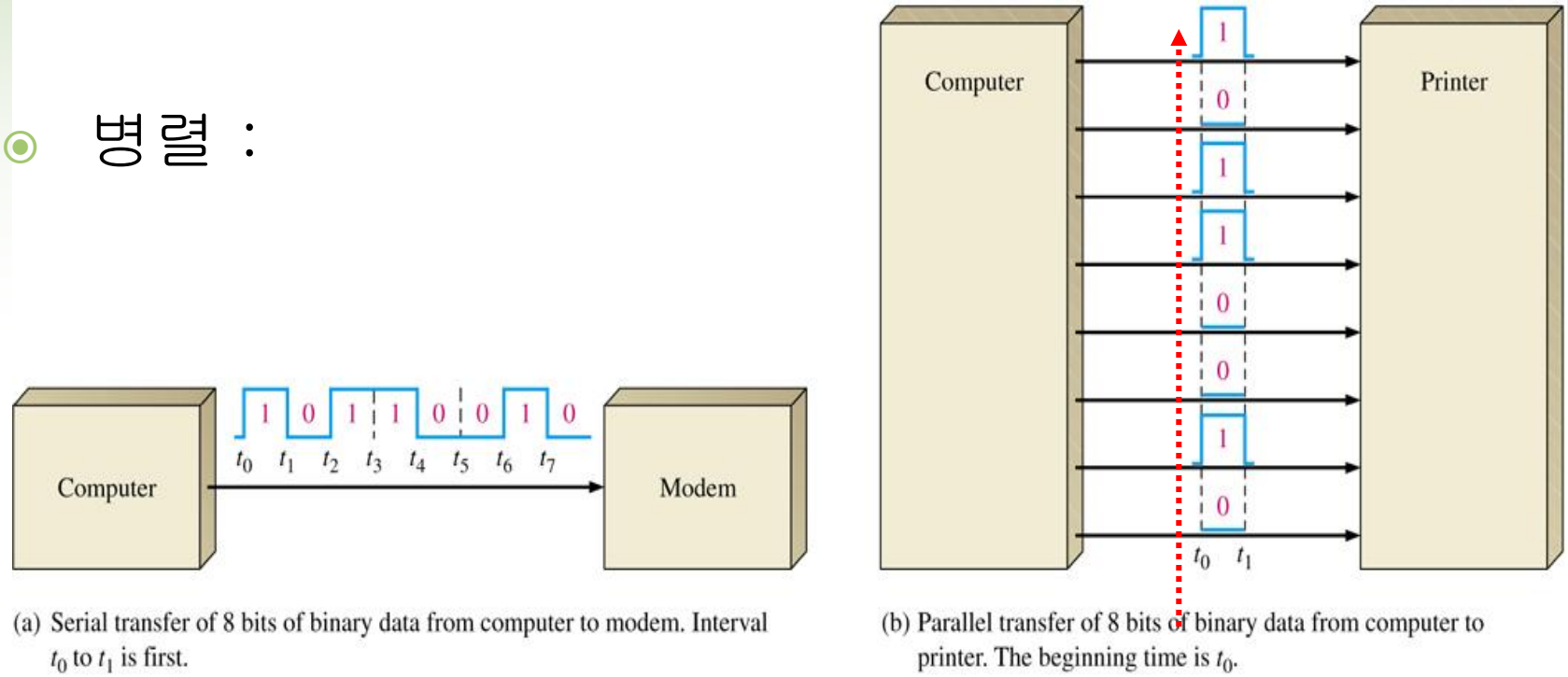


Figure 1-11 Example of a timing diagram

데이터 전송(Data Transfer)

- 직렬 :
- 병렬 :

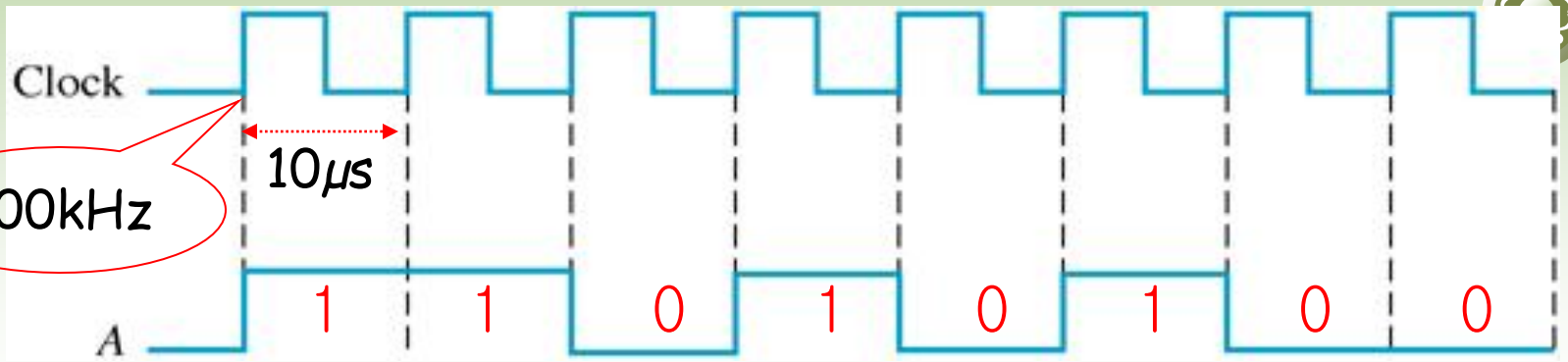


(a) Serial transfer of 8 bits of binary data from computer to modem. Interval t_0 to t_1 is first.

(b) Parallel transfer of 8 bits of binary data from computer to printer. The beginning time is t_0.

Figure 1-12 Illustration of serial and parallel transfer of b inary data. Only the data lines are shown.

예제1-2



(a) 100kHz 클럭을 사용할 때, 8비트 직렬전송에 필요한 시간과 비트열을 구하라.

=>

=>

(b) 병렬전송에 필요한 시간을 구하라.

=>

논리 연산의 기초

- 불 대수(Boolean algebra)
  - George Boole이 1854년 논리식을 다루기 위하여 창안한 대수학.

- 기본 논리 연산과 심볼

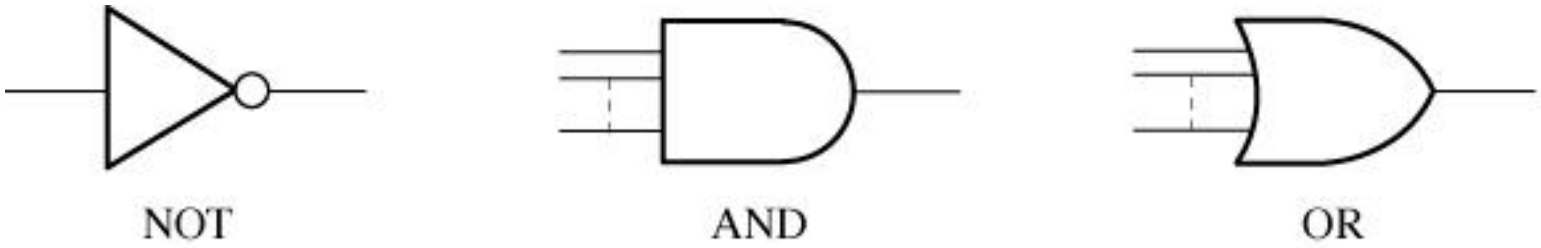
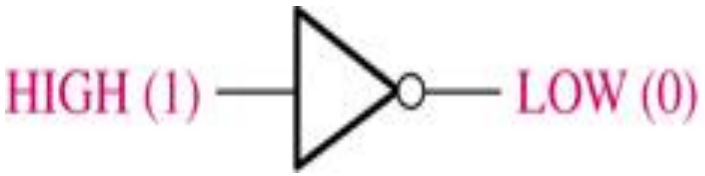
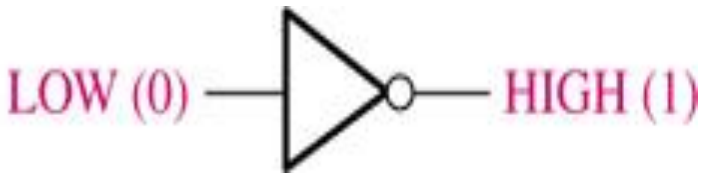


Figure 1-15 The basic logic operations and symbols.

NOT, AND, OR

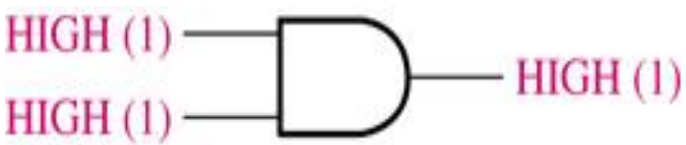
- NOT 연산

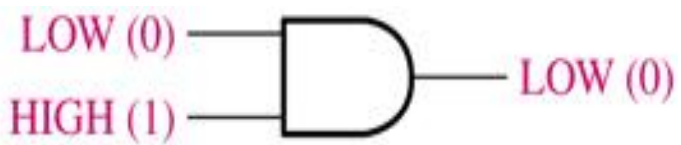


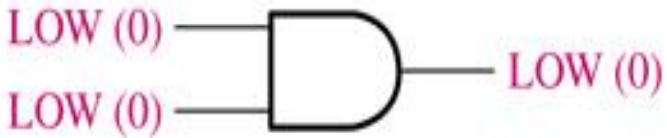


NOT, AND, OR

- AND 연산







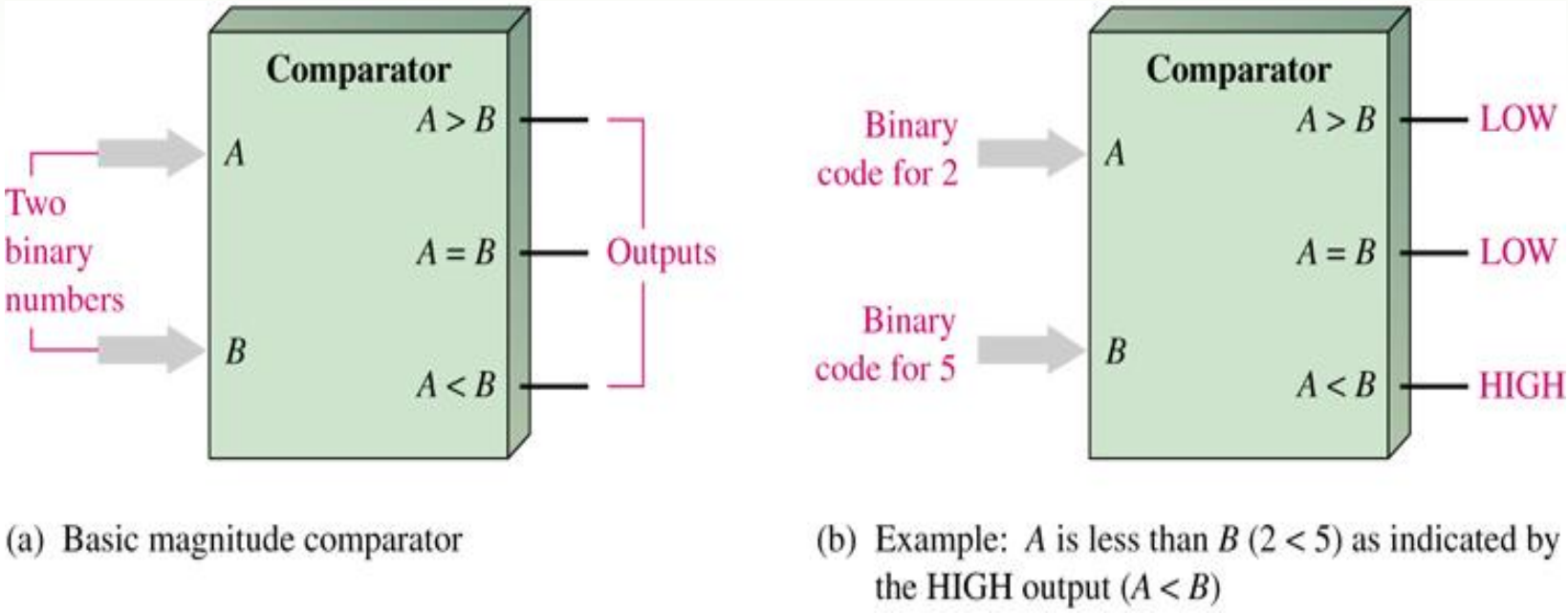
NOT, AND, OR

- OR 연산

논리 함수의 기초

- 논리 함수(Logic functions)

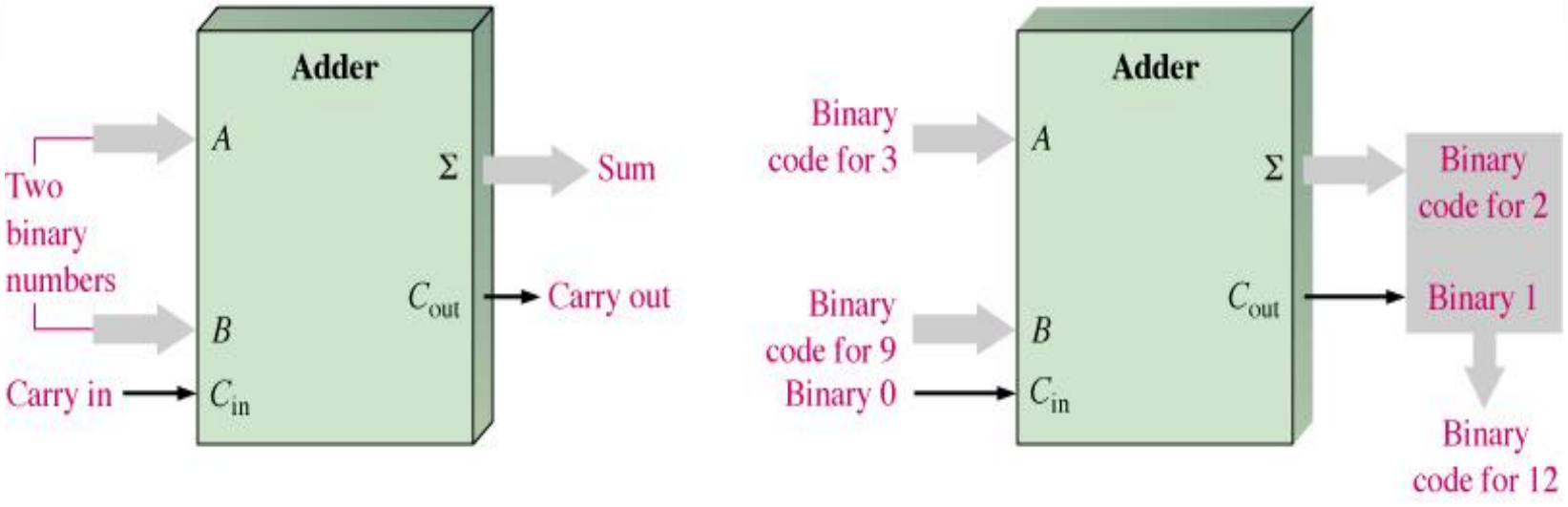
비교함수(The Comparison Func.)



(a) Basic magnitude comparator

(b) Example: A is less than B ($2 < 5$) as indicated by the HIGH output ($A < B$)

산술함수(The Arithmetic Func.)

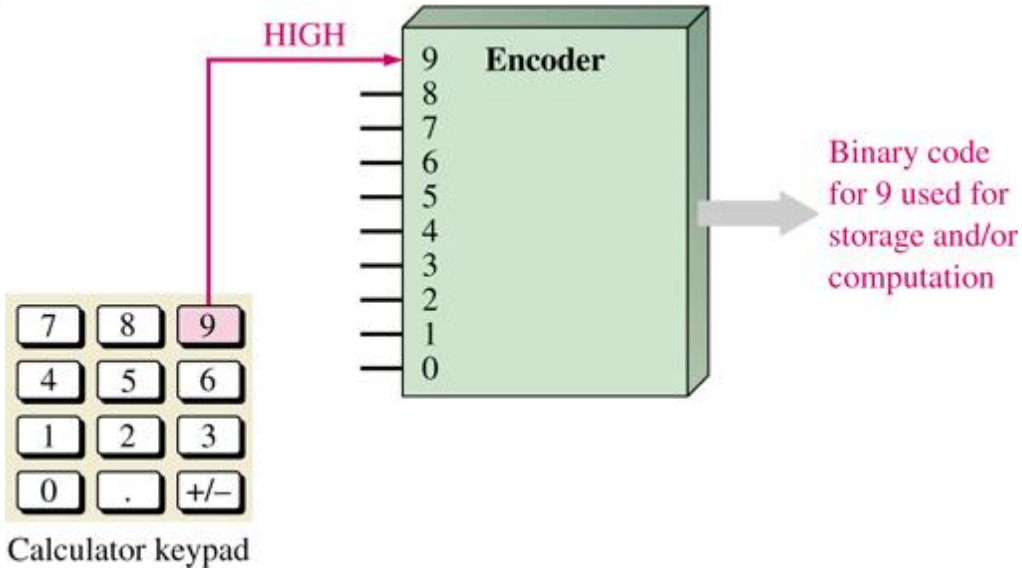


(a) Basic adder

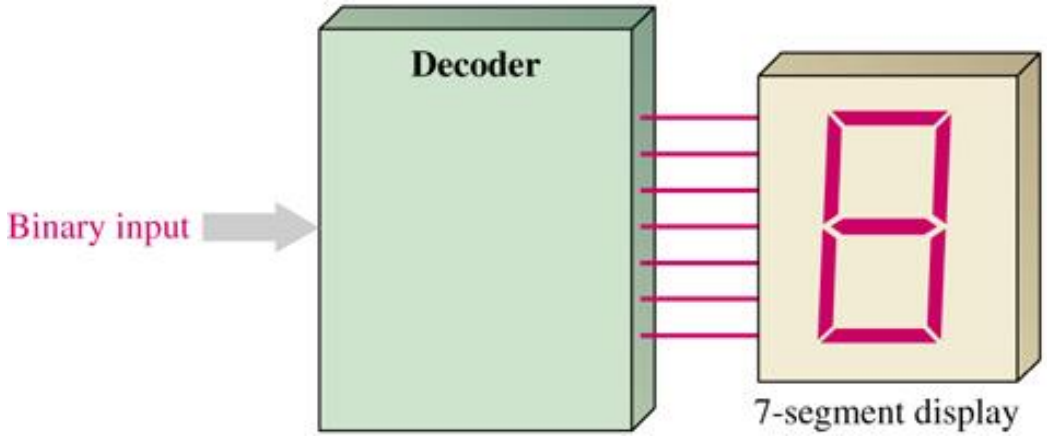
(b) Example: *A* plus *B* (3 + 9 = 12)

코드변환함수(The Code Conversion Func.)

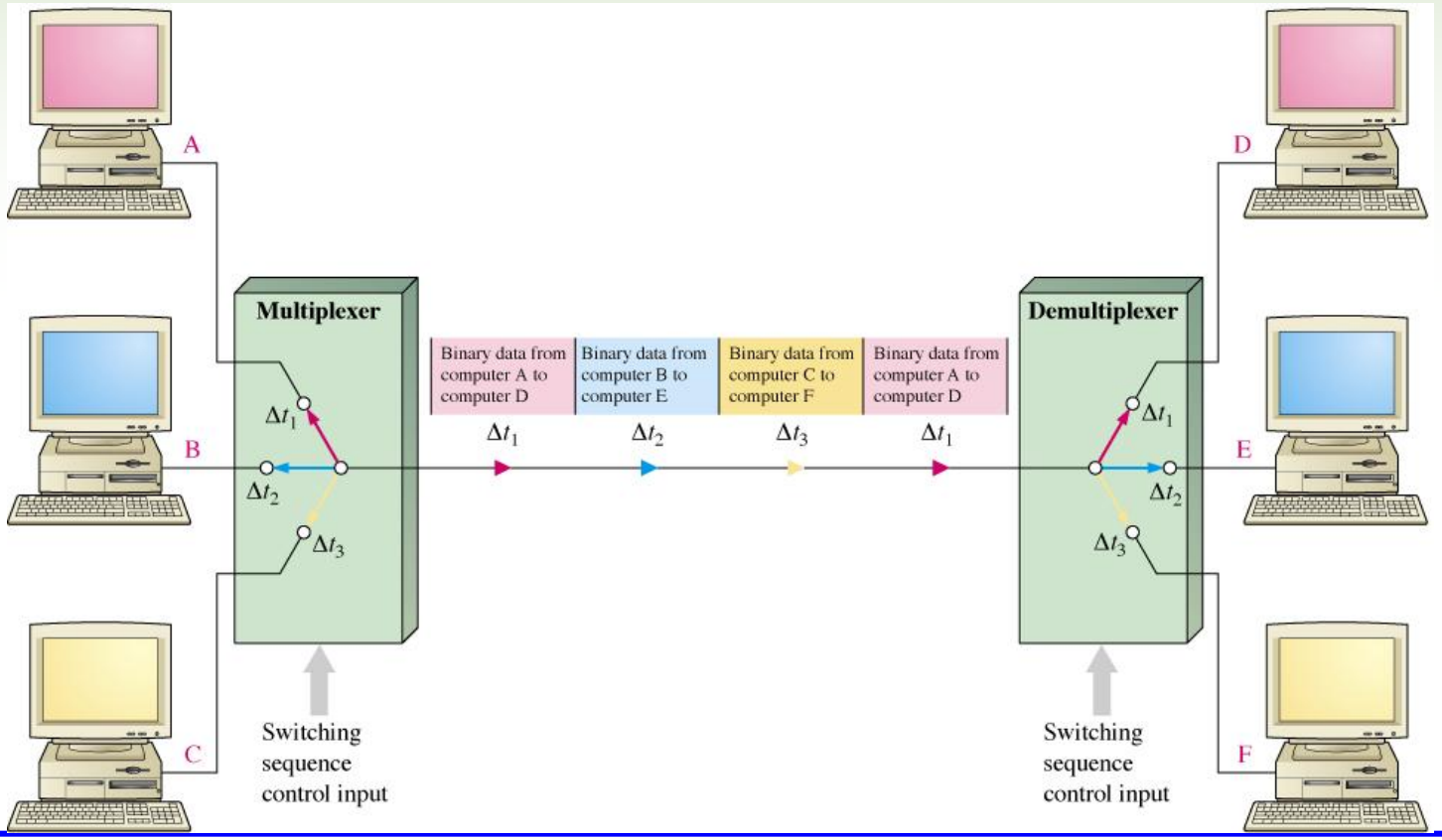
인코딩함수(The Encoding Func.)



디코딩함수(The Decoding Func.)



데이터 선택함수(The Data Selection Func.)



저장함수(The Data Storage Func.)

- 플립-플롭(Flip-flops)
- 레지스터(Registers)
- 반도체 메모리(Semiconductor Memories)
  ROM(Read Only Memory), RAM(Random Access Memory)
- 자기 메모리(Magnetic Memories)
  플로피 디스크, 하드 디스크 등

레지스터

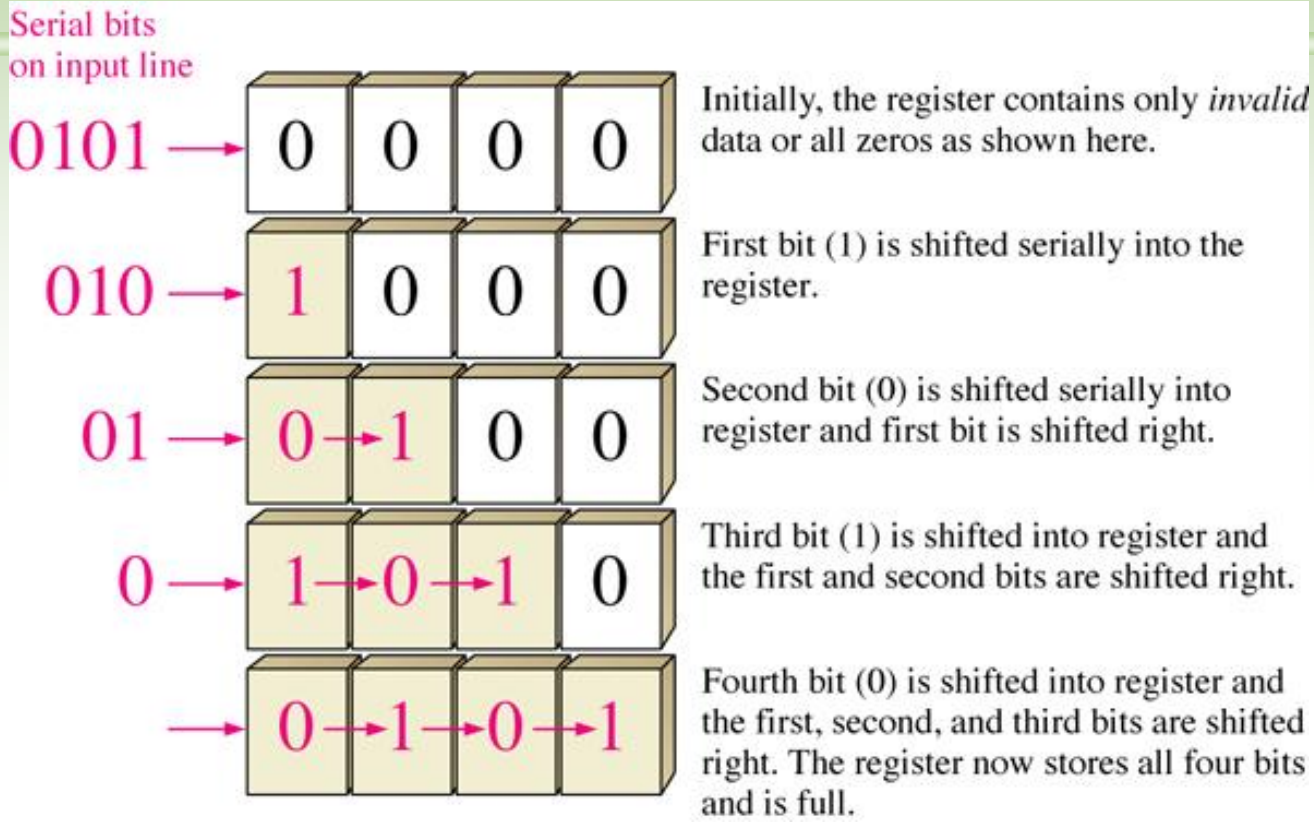


Figure 1-24 Example of the operation of a 4-bit serial shift register. Each block represents one storage "cell" or flip-flop.

레지스터

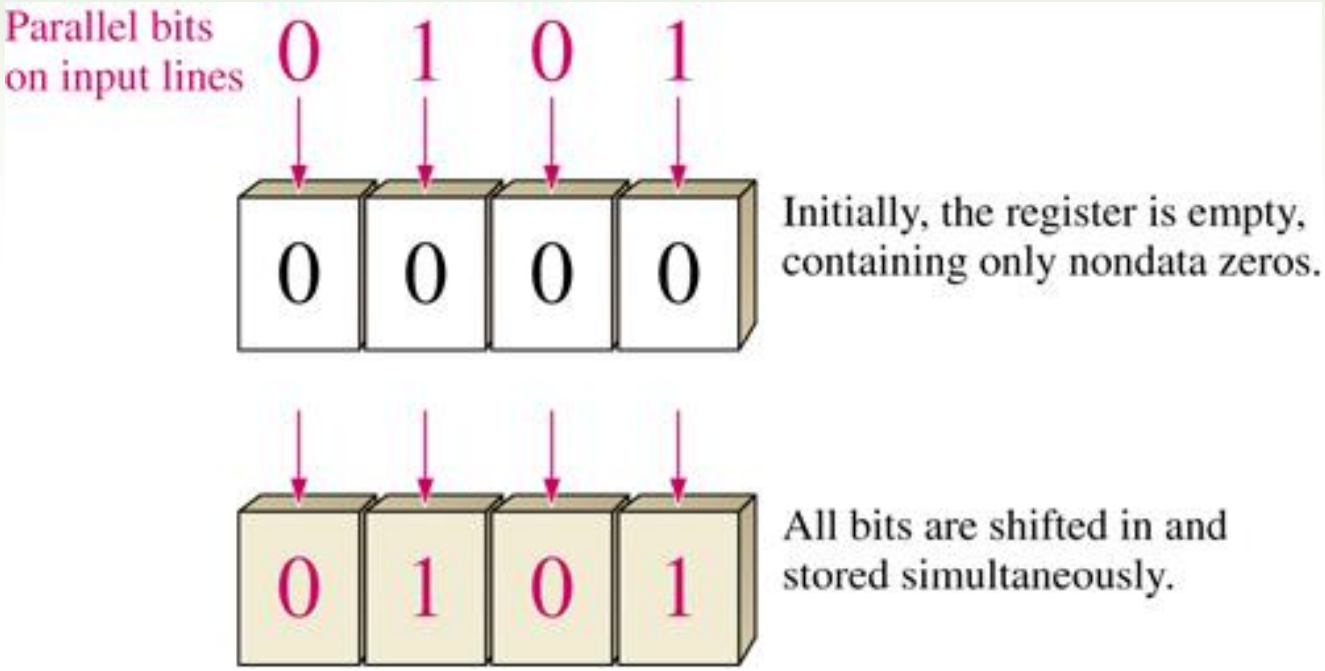


Figure 1-25 Example of the operation of a 4-bit parallel shift register.

계수 함수(The Counting Func.)

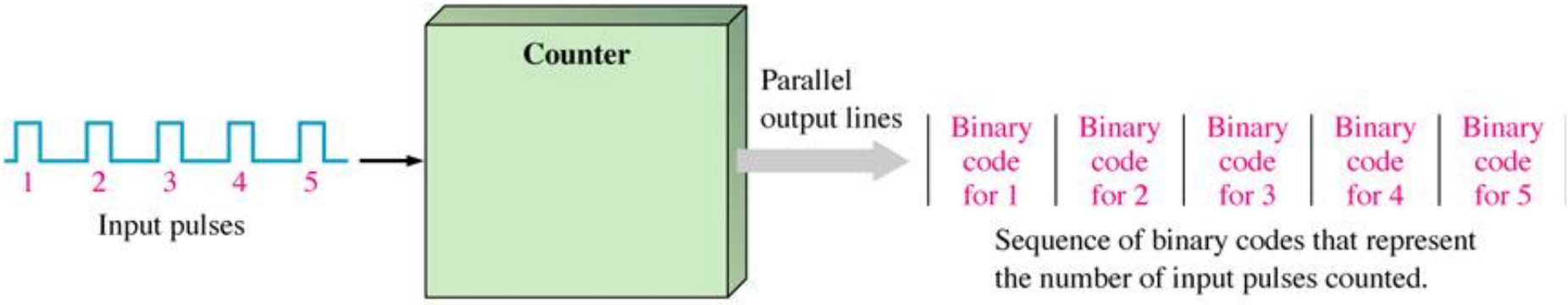


Figure 1-26 Illustration of basic counter operation.

시스템 응용에서의 기초적인 논리함수

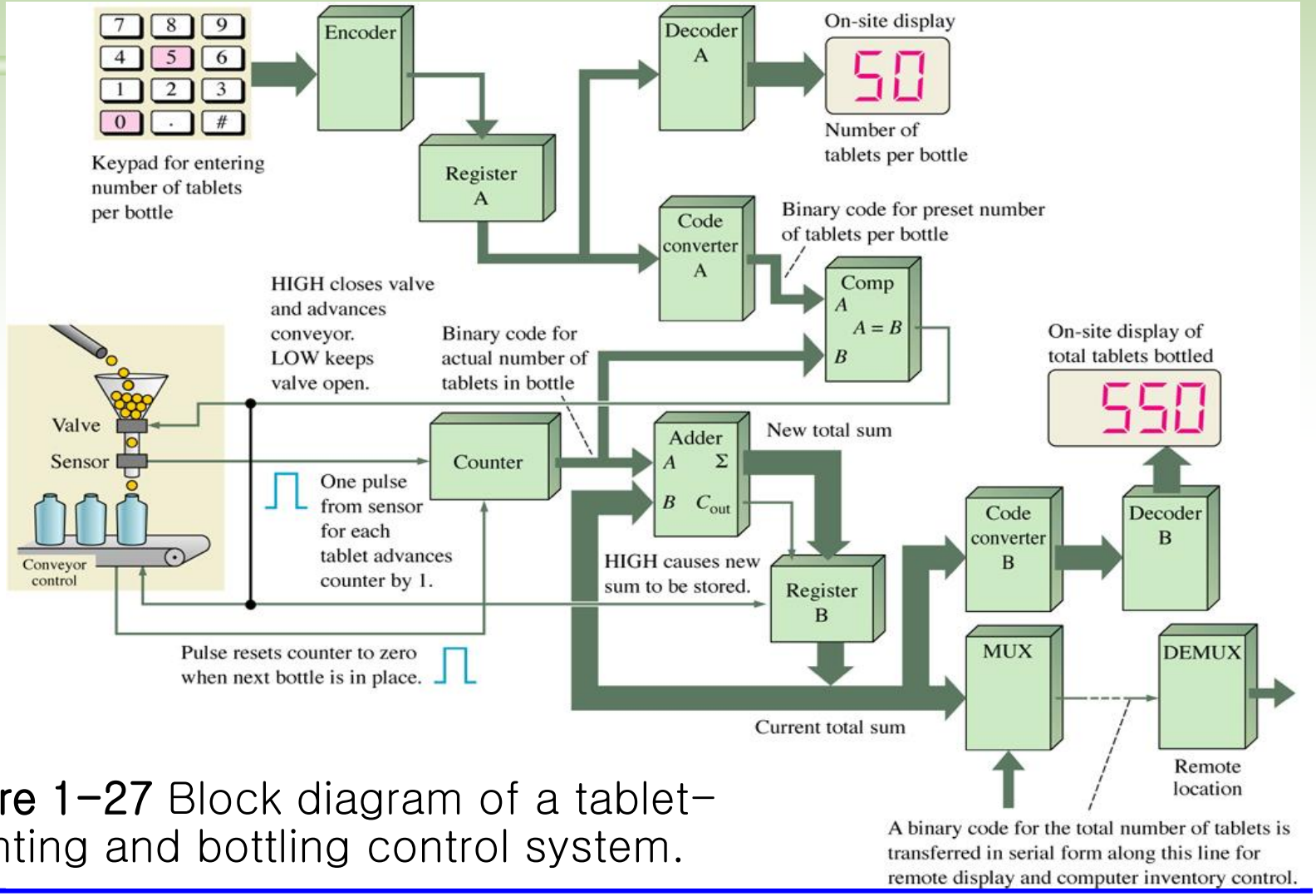


Figure 1–27 Block diagram of a tablet-counting and bottling control system.

고정-기능 집적회로(Fixed-func. Integrated Circuit)

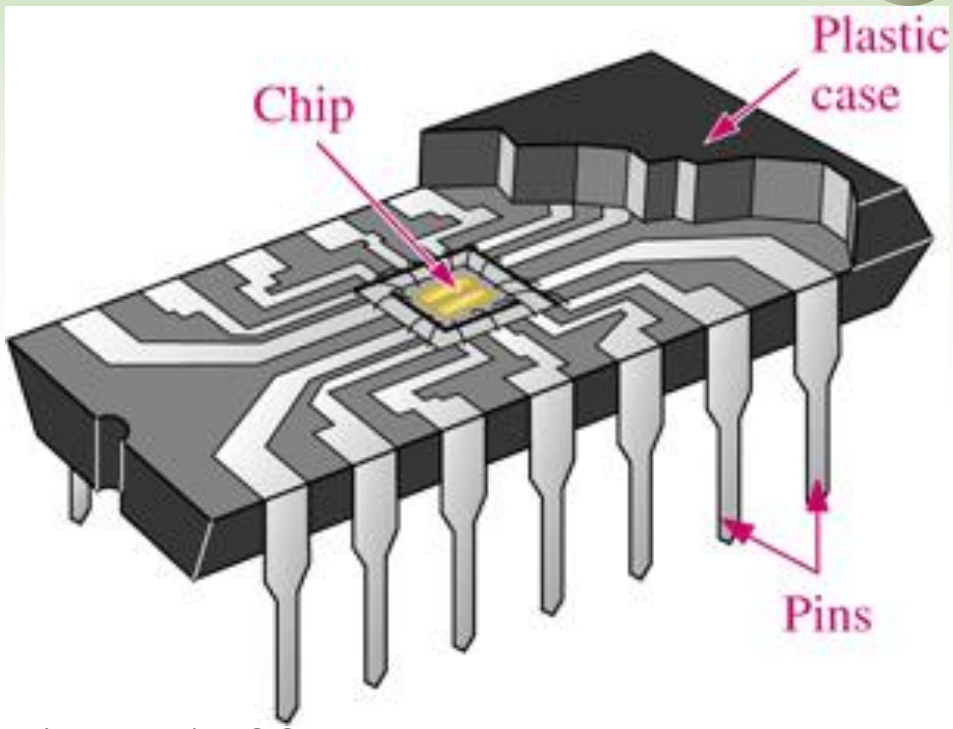
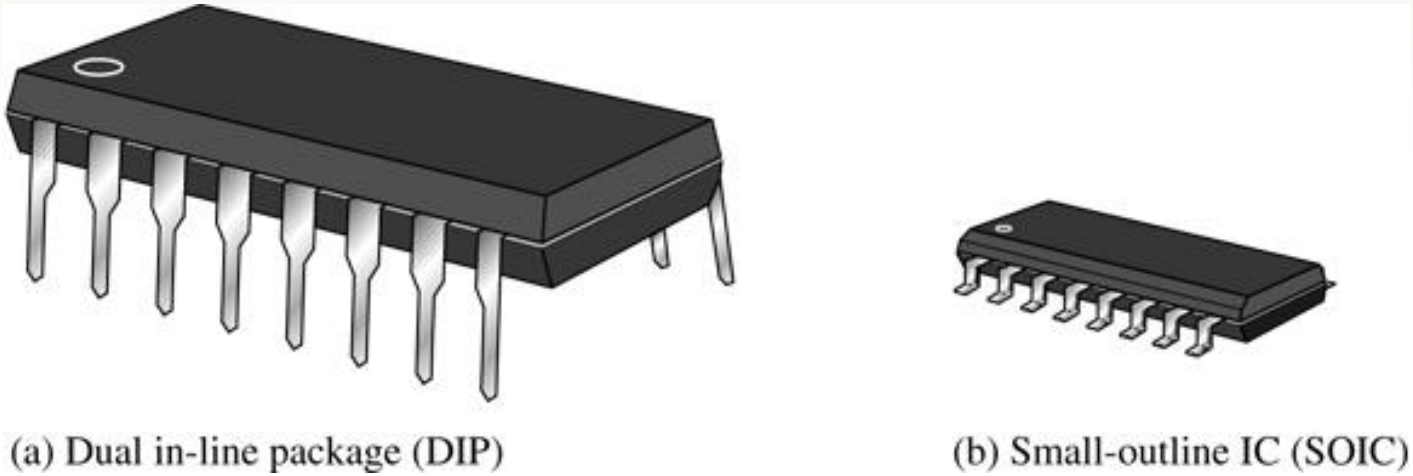


Figure 1-28 Cutaway view of one type of fixed-function IC package showing the chip mounted inside, with connections to input and output pins.

IC패키지(IC Packages)

- Through-hole mounted
- Surface mounted



(a) Dual in-line package (DIP)

(b) Small-outline IC (SOIC)

Figure 1-29 Examples of through-hole and surface-mounted devices. The DIP is larger than the SOIC with the same number of leads. This particular DIP is approximately 0.785 in. long, and the SOIC is approximately 0.385 in. long.

표면실장 패키지(Surface-Mount Pakages)

SMT 패키지의 종류 ;

SOIC, PLCC, LCCC, Flat pack

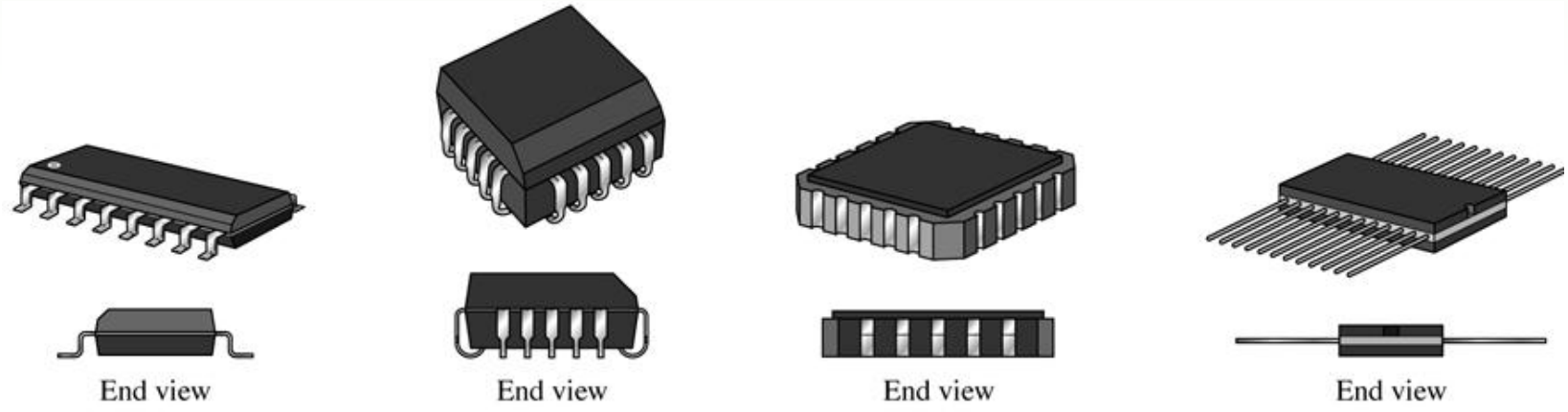


Figure 1-30 Examples of SMT package configurations

IC 핀 번호 붙이기 규칙

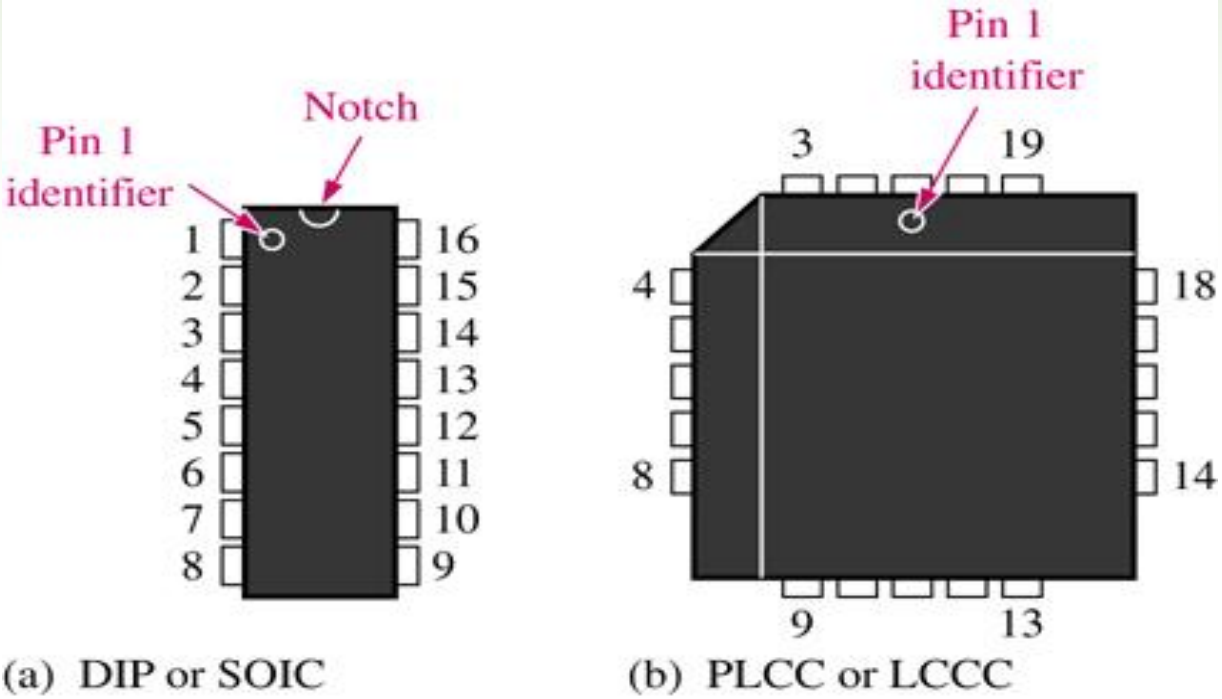


Figure 1-31 Pin numbering for two standard types of IC packages. Top views are shown.

고정-기능 IC의 복잡도 분류

- Small-scale integration(SSI)

  하나의 칩에 12개의 등가게이트까지 가짐.
  기본적인 게이트들과 플립-플롭 포함

- Medium-scale integration(MSI)

  하나의 칩에 12 ~ 99개의 등가게이트까지 가짐
  인코더, 디코더, 카운터, 레지스터, MUX, 산술회로, 작은 메모리 등을 포함

- Large-scale integration(LSI)

  하나의 칩에 100 ~ 9,999개의 등가게이트까지 가짐

- Very large-scale integration(VLSI)

  하나의 칩에 100,000 ~ 99,999개의 등가게이트까지 가짐

- Ultra large-scale integration(ULSI)

  하나의 칩에 1000,000 개 이상의 등가게이트를 가짐

집적회로 기술(IC Technologies)

- 바이폴러 접합 트랜지스터
  (BJT; Bipolar Junction Transistor)

  TTL(Transistor-transistor logic)
  ECL(Emitter-coupled logic)

- MOSFET(Metal-oxide Semiconductor
  Field-effect Transistor)

  CMOS(Complementary MOS)
  NMOS(N-channel MOS)

프로그래머블 논리 (Programmable Logic)

- PLD(Programmable Logic Device) :

- PLD의 장점

PLD의 형태

- SPLD(Simple Programmable Logic Devices)
  - 여러 개의 SSI 또는 MSI 장치를 대체할 수 있음
  - PAL, GAL, PLA, PROM
- CPLD(Complex Programmable Logic Devices)
  - 2~64개의 SPLD의 성능
  - 44 ~ 160 핀
- FPGA(Field-programmable Gate Arrays)
  - 64개 ~ 수천개의 논리 배열 블록으로 구성
  - 최대의 논리 용량을 가짐

고정-기능 논리 접근 방법

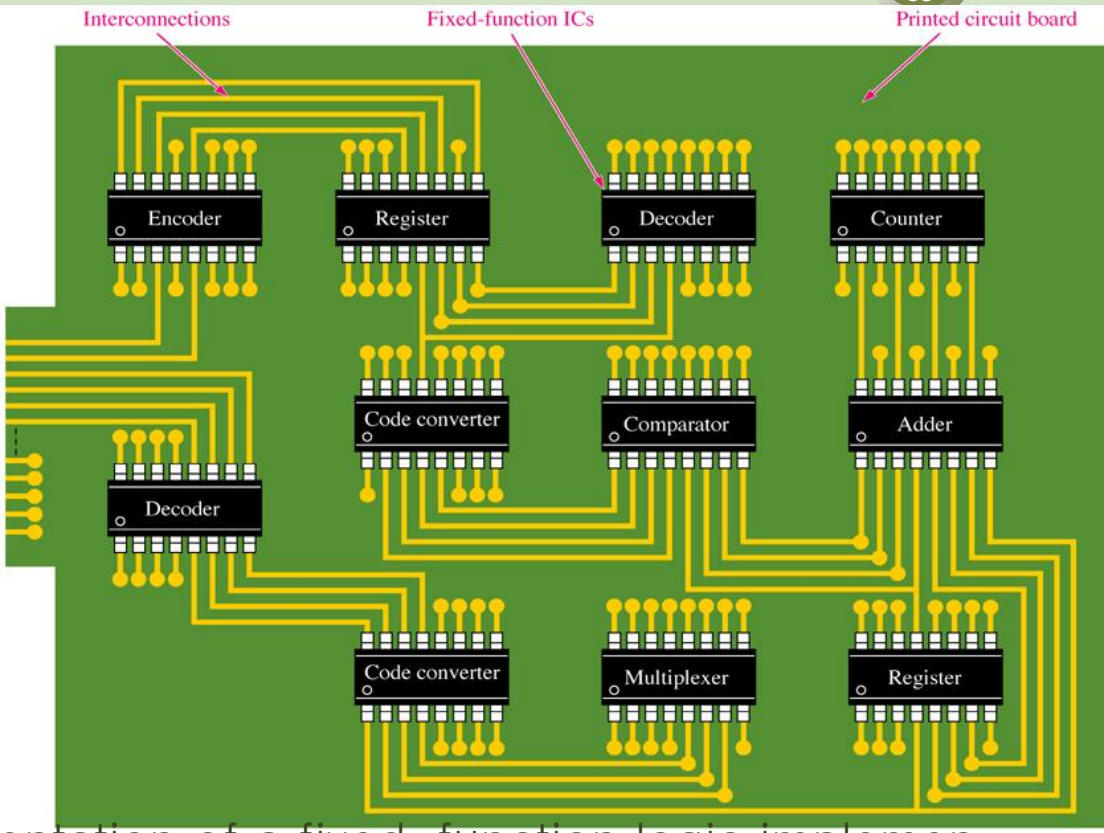


Figure 1-34 A simplified representation of a fixed-function logic implementation of the system in Figure 1-27. A few interconnections are arbitrarily shown for illustration only.

프로그래머블 논리 접근방법